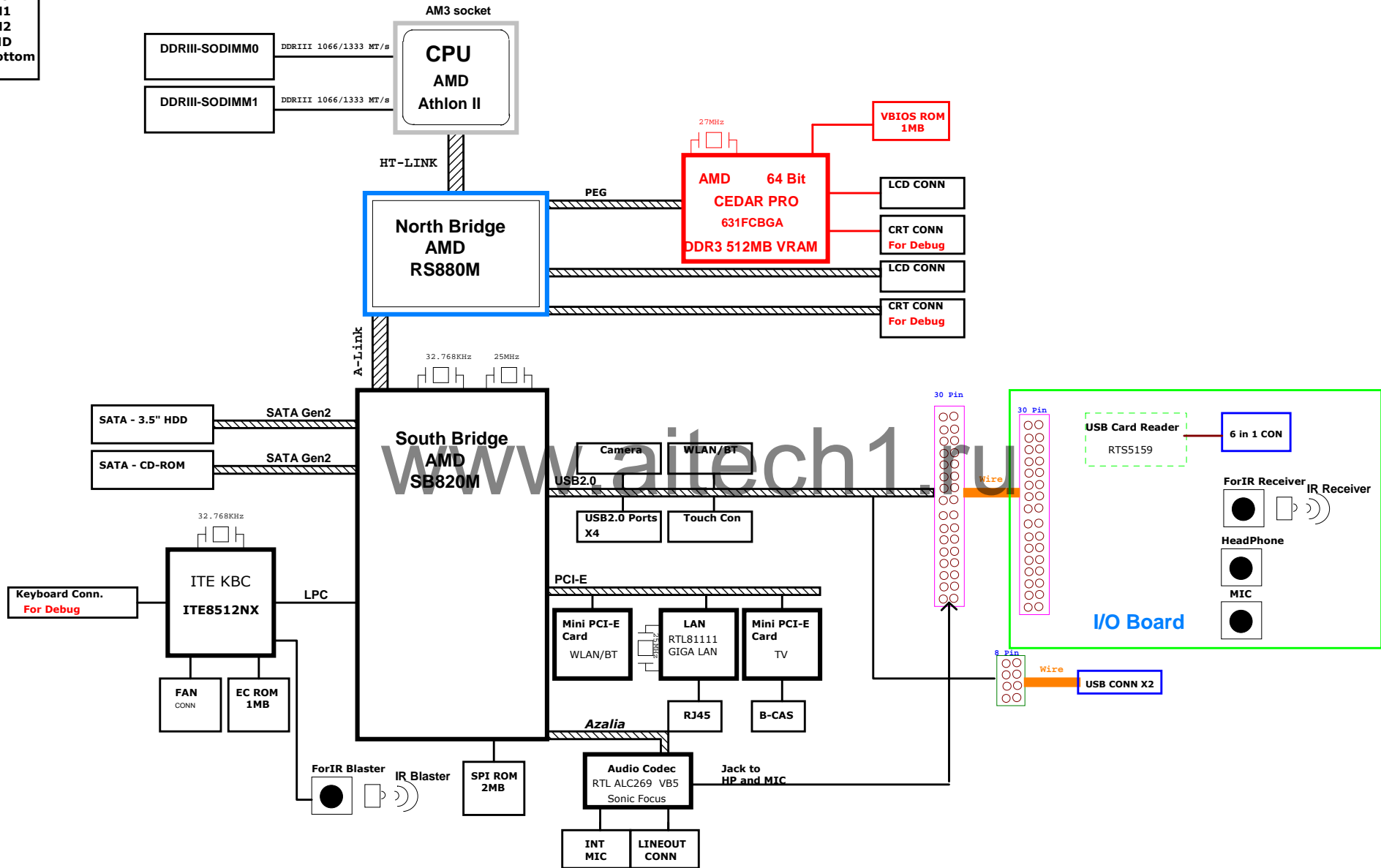


PCB STACK UP

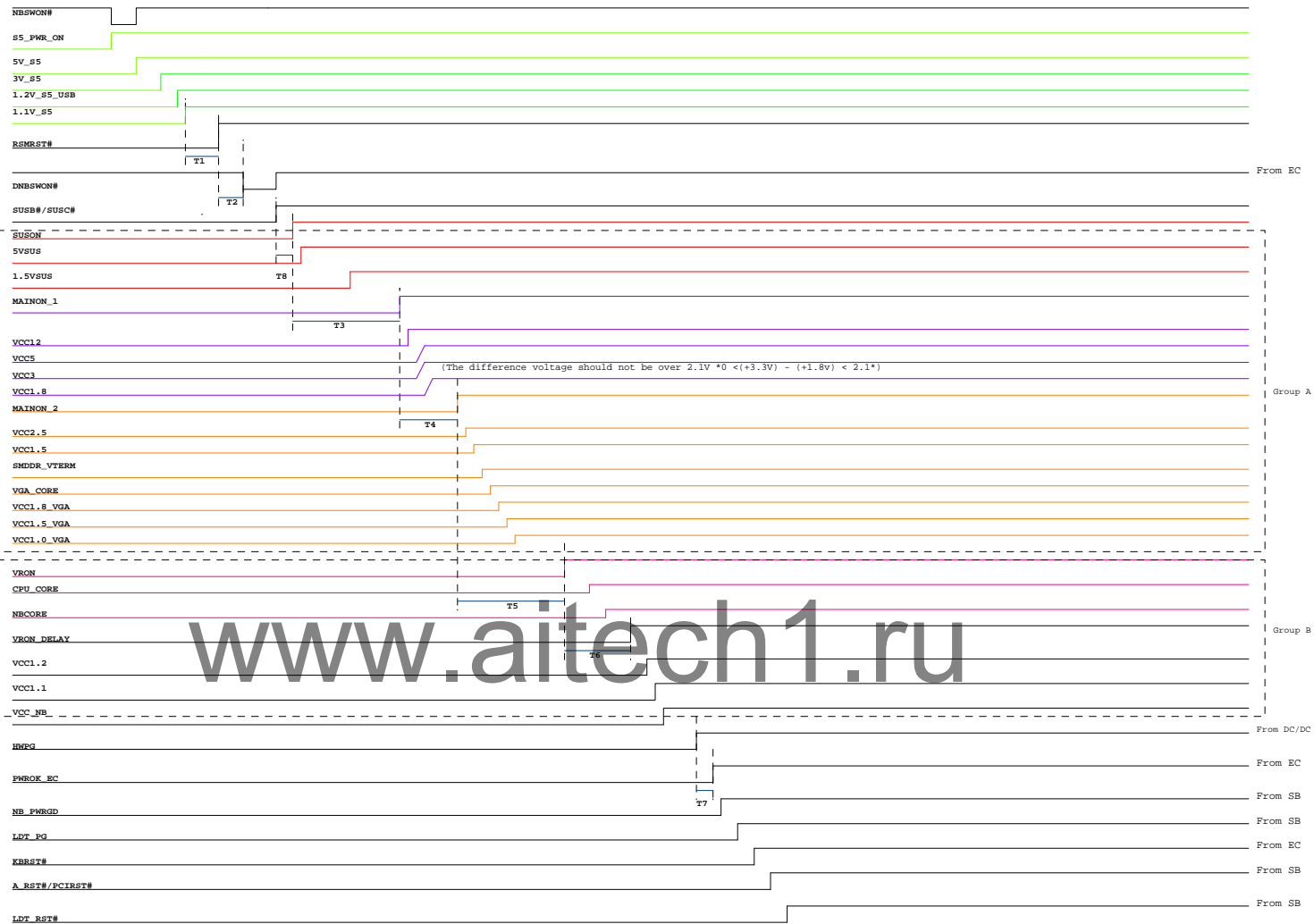
LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : Bottom

Shasta_NZ2 BLOCK DIAGRAM

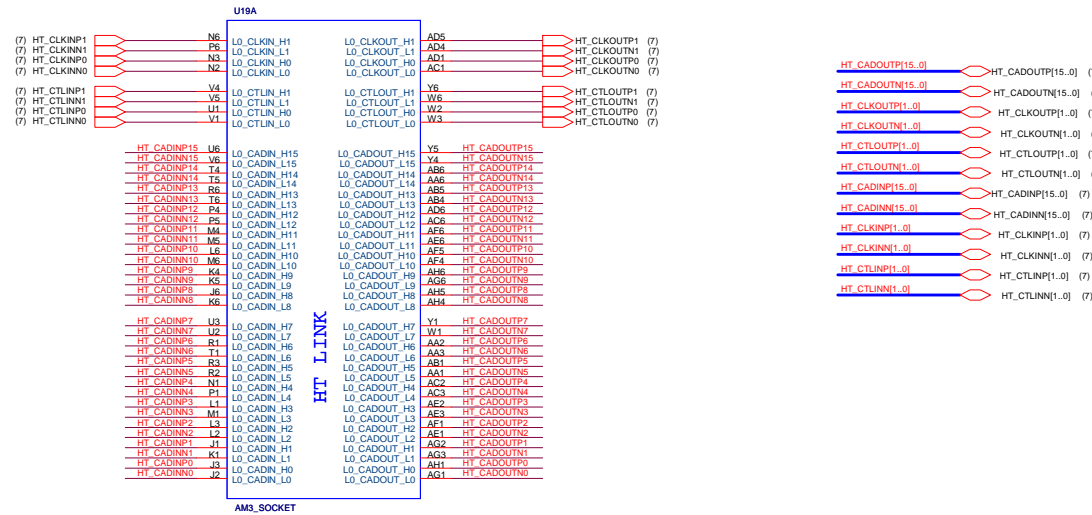


- 01--SYSTEM BLOCK DIAGRAM
 02--PAGE SHEET & POWER SEQUENCE
 03--AM3 CPU HT & DEBUG
 04--AM3 CPU MEMORY
 05--AM3 CPU CONTROL & MISC
 06--AM3 CPU PWR & GND
 07--RS880M-HT LINK I/F
 08--RS880M-PCIE I/F
 09--RS880M-SYSTEM I/F
 10--RS880M-SPMEM/STRAPS
 11--RS880M-POWER
 12--SB820M-PCIE/PCI/CPU/LPC
 13--SB820M-ACPI/GPIO/USB
 14--SB820M-SATA/IDE/HWM/SPI
 15--SB820M-PWR/DECOUPLING
 16--SB820M-STRAPS/PWRGD
 17--DDR3 CHA DIMM 0
 18--DDR3 CHB DIMM 1
 19--CEDAR-S3_PCIE Interface
 20--CEDAR-S3_Main
 21--CEDAR-S3_GND / LVDS/ Straps
 22--CEDAR-S3_Power_and_NC
 23--CEDAR-S3/MEM Interface
 24--CEDAR_VRAM (DDR3 BGA96)
 25--Panel (LVDS)
 26--EC ITE 8512N/FLASH
 27--Audio Codec(ALC269)
 28--LAN RTL8111
 29--SATA HDD/ODD/FAN/HOLE
 30--MINI PCIE (WLAN/TV/IR/IO)
 31--USB/CCD/TOUCH/CRT
 32--AMD AM3 CPUCORE(NCP5293)
 33--CPU DRIVER
 34--NBCORE (RT8209A), 1.1V_S5
 35--System +5V/+3V (RT8206B)
 36--DDR_1.5VSUS (TPS51116)
 37--VGACORE (RT8208/1.8V)
 38--LDO/VDDA/+1.8V/0.9V
 39--ACIN/+12V(NCP1589A)
 40--DISCHARGE
 41--CHANGE LIST

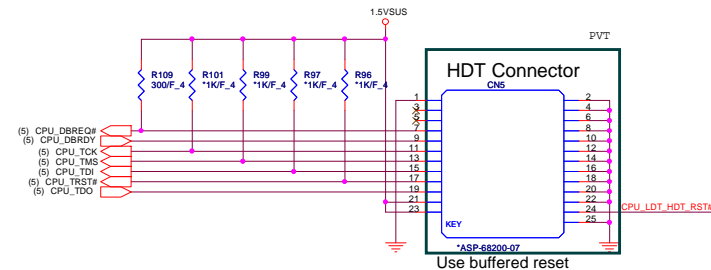
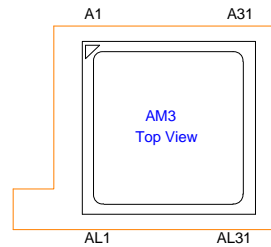
NZ2 AM3 platform Power on Sequence



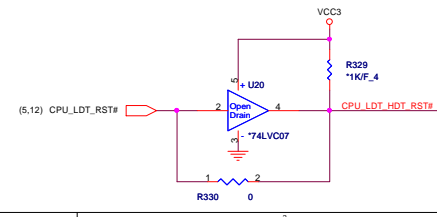
T1: S5_PWR_ON to RSMRST# 20ms
 T2: RSMRST# to DNBSWON# 50ms
 T3: SUSON to MAINON_1 5ms
 T4: MAINON_1 to MAINON_2 2ms
 T5: MAINON_2 to VRON 30ms
 T6: VRON to VRON_DELAY 12ms
 T7: HWPG to PWROK_EC 30ms
 T8: SUSB#/SUSC# to SUSON 10ms



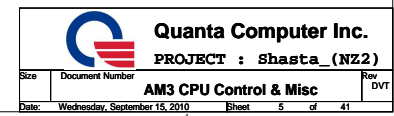
www.aitech1.ru

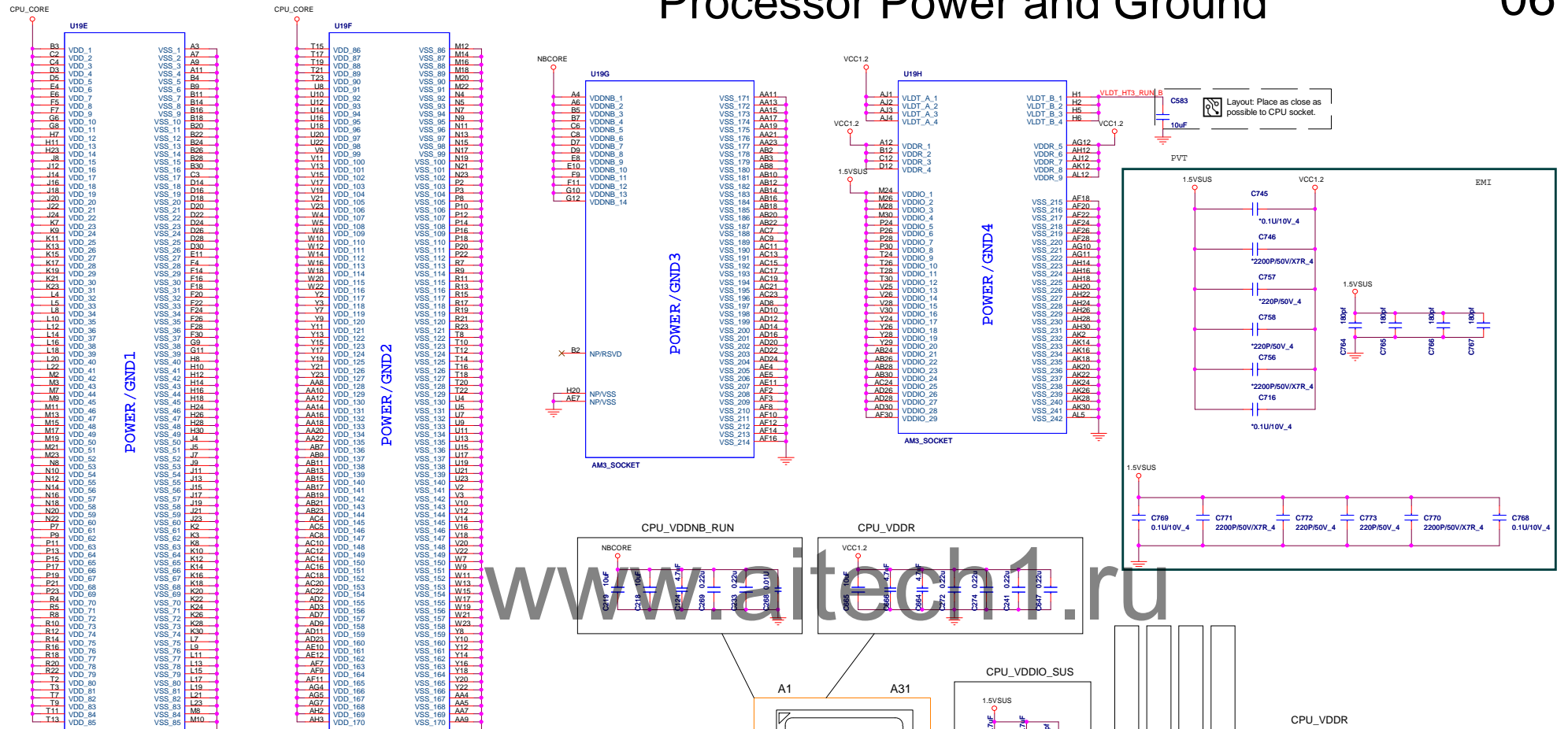


HDT Header

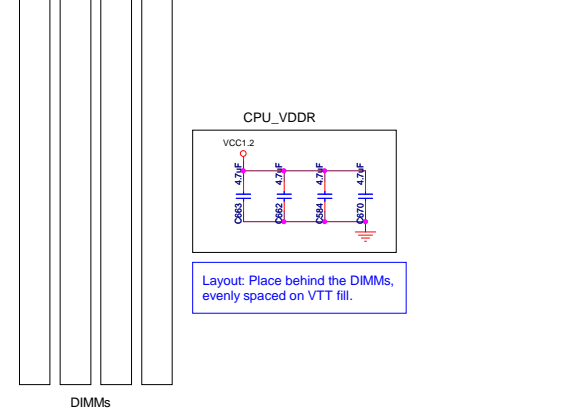
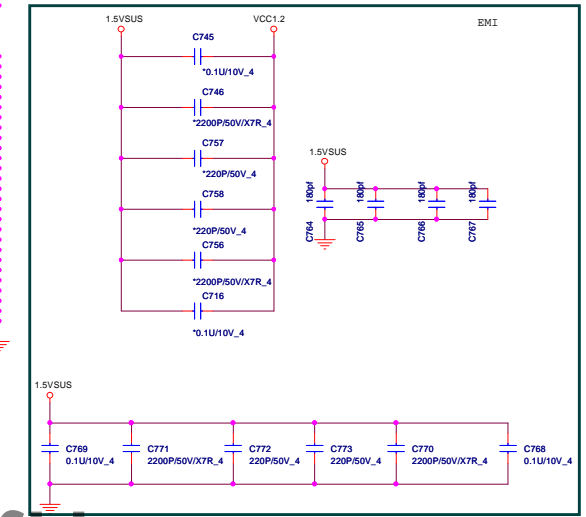
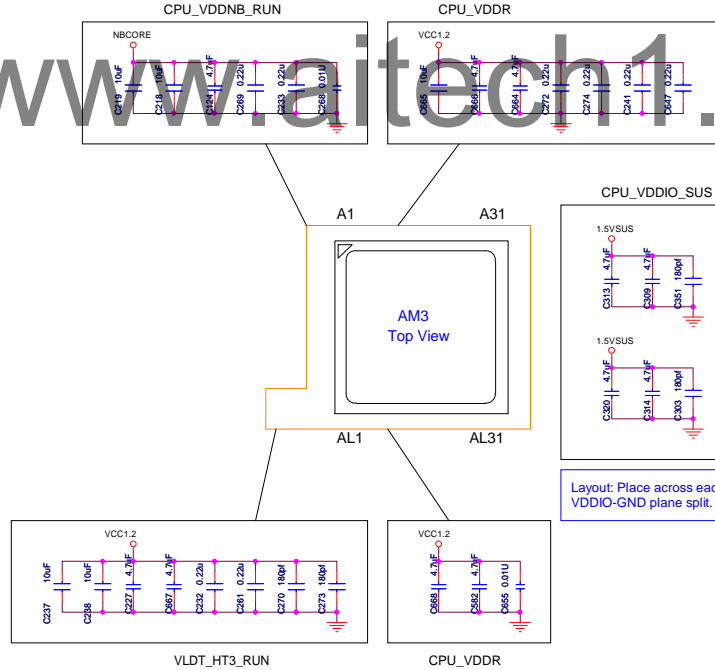
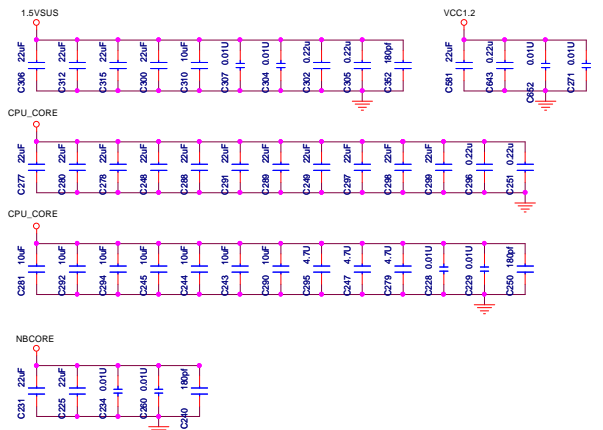


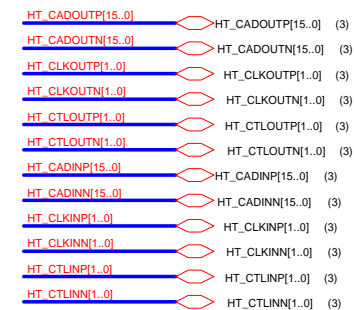
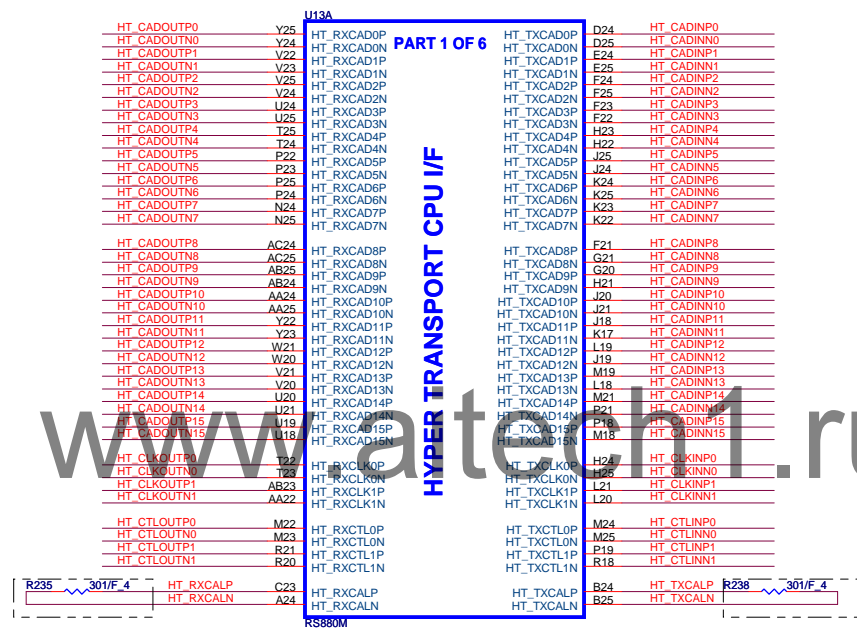
05





Bottom Side Decoupling





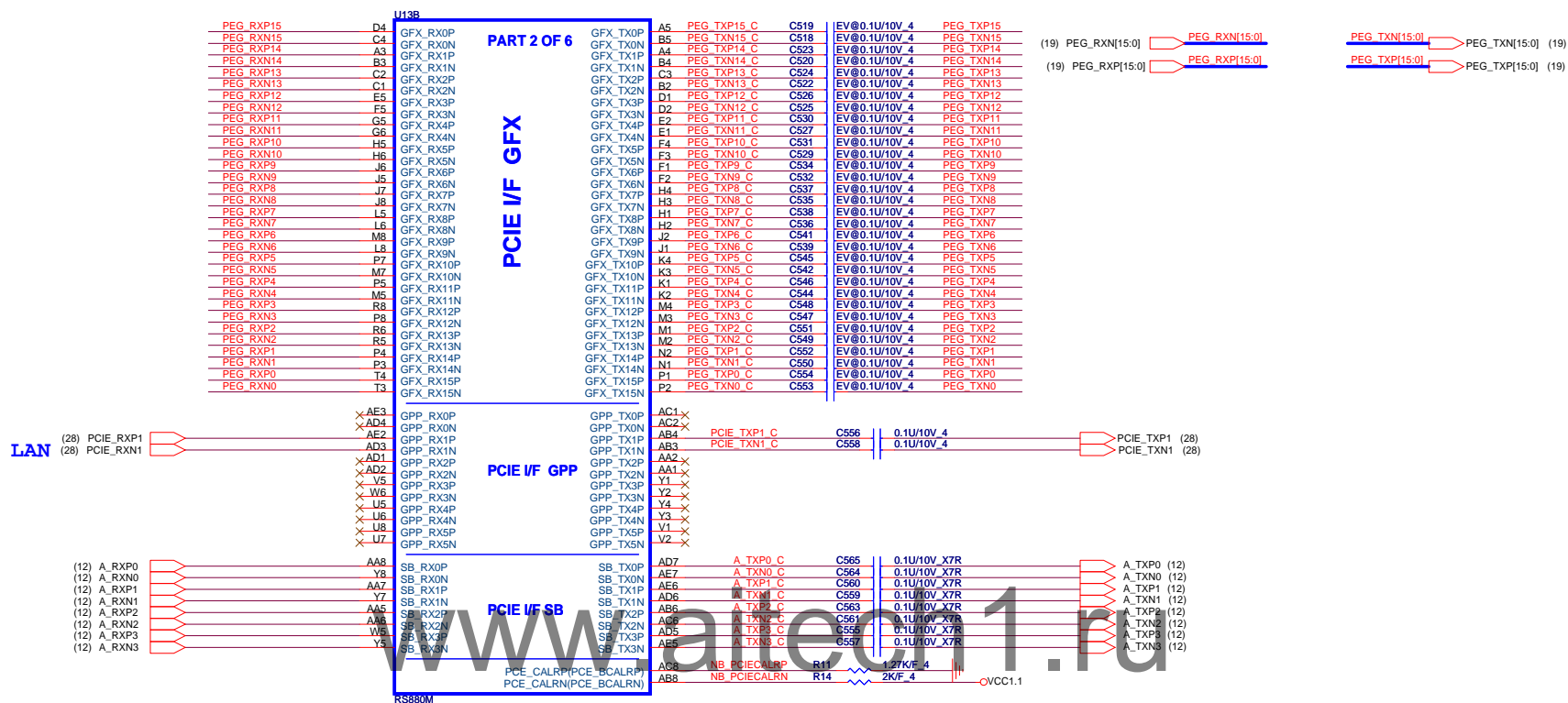
signals	RS880M
HT_TXCALP	R7349 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R7350 301 ohm 1%
HT_RXCALN	

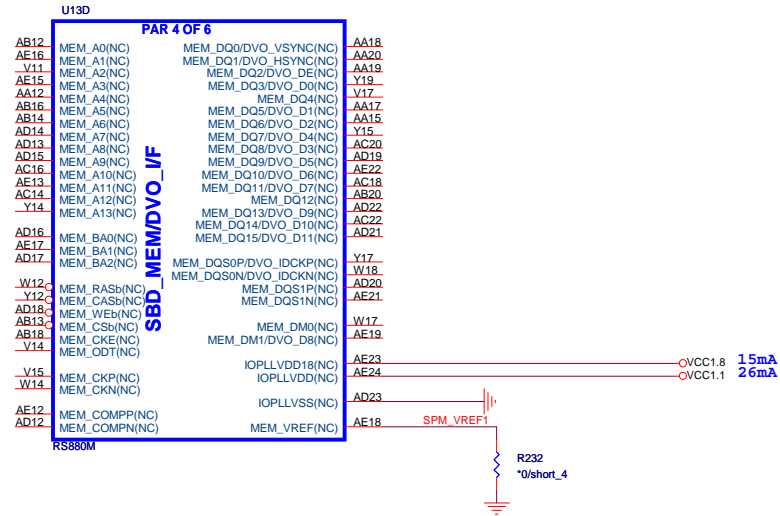


Quanta Computer Inc.

PROJECT : Shasta_(NZ2)

Size	Document Number	Rev
	RS880M-HT Link I/F	DVT
Date:	Wednesday, September 15, 2010	Sheet 7 of 41





STRAP_DEBUG_BUS_GPIO_ENABLE#

Enables the Test Debug Bus using GPIO

RS880M	
1 Disable	
0 Enable	

DFT_GPIO1: LOAD_EEPROM_STRAPS

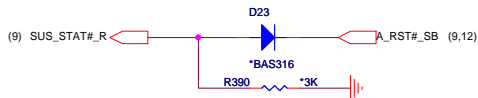
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



Quanta Computer Inc.

PROJECT : Shasta_(NZ2)

RS880M-Spmem/Straps

Size Document Number Rev DVT

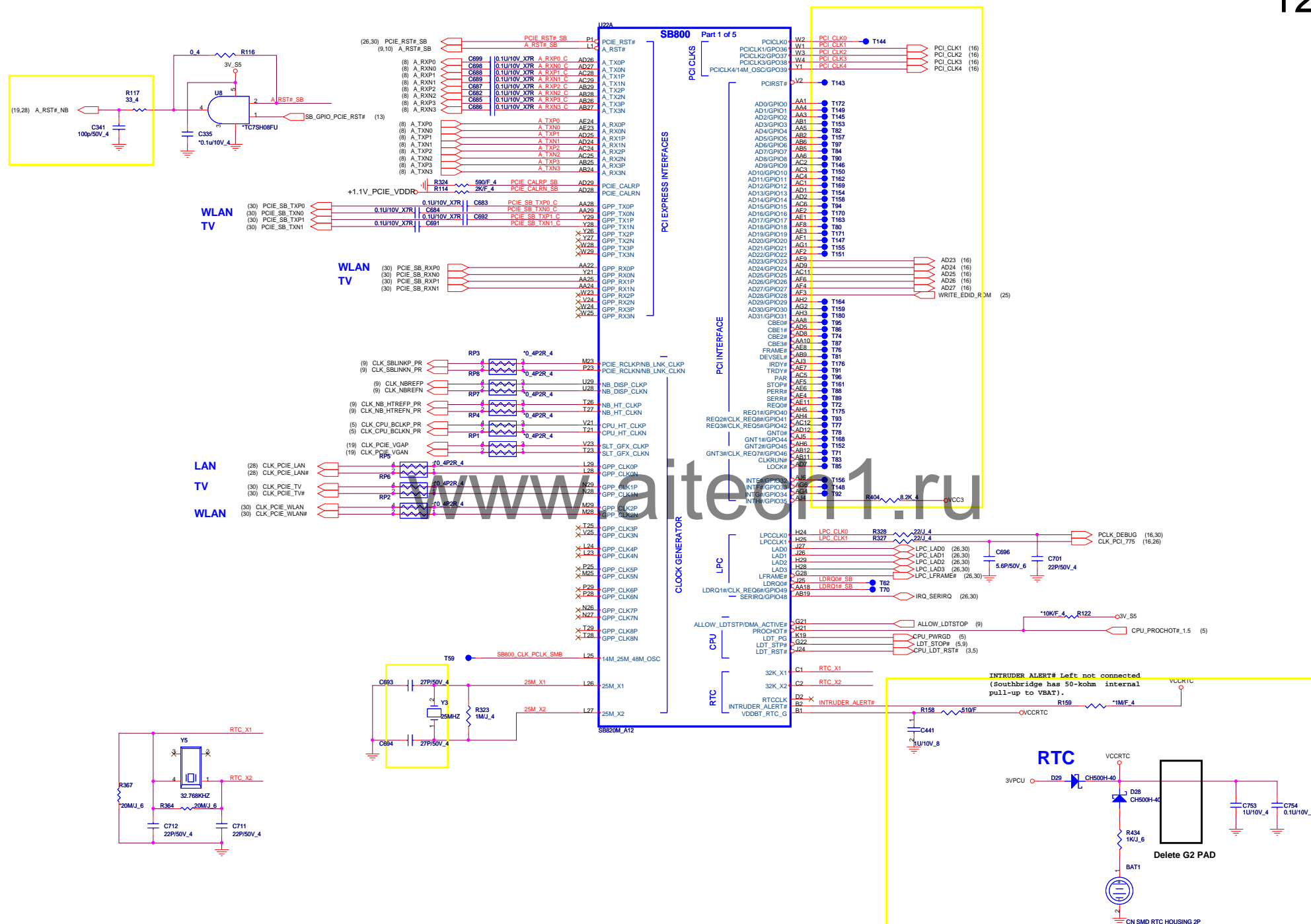
Date: Wednesday, September 15, 2010 Sheet 10 of 41

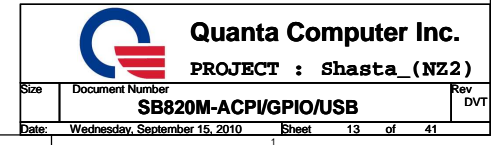
The diagram illustrates a 100-pin connector layout. The pins are organized into two main sections: pins 1-50 on the left and pins 51-100 on the right. The left section is labeled 'PART 66' and the right section is labeled 'GROUND'. The pins are connected to various components, including a 100-pin connector, a 100-pin connector, and a 100-pin connector. The diagram also shows a 100-pin connector with pins 1-100. The pins are connected to various components, including a 100-pin connector, a 100-pin connector, and a 100-pin connector.

Pin	Signal	Pin	Signal
A25	VSSAHT1	L12	VSS11
D21	VSSAHT2	M14	VSS12
G22	VSSAHT3	N13	VSS13
G24	VSSAHT4	P12	VSS14
G25	VSSAHT5	R11	VSS15
H19	VSSAHT6	T11	VSS16
L17	VSSAHT7	T12	VSS18
L22	VSSAHT8	U14	VSS19
L24	VSSAHT9	VSS20	VSS20
P25	VSSAHT10	W15	VSS21
P26	VSSAHT11	W16	VSS22
N22	VSSAHT12	VSS23	VSS23
P20	VSSAHT13	VSS24	VSS24
R19	VSSAHT14	VSS25	VSS25
R21	VSSAHT15	VSS26	VSS26
R25	VSSAHT16	VSS27	VSS27
H20	VSSAHT17	VSS28	VSS28
H22	VSSAHT18	VSS29	VSS29
U22	VSSAHT19	VSS30	VSS30
V19	VSSAHT20	AE20	VSS31
W24	VSSAHT21	VSS32	VSS32
W25	VSSAHT22	VSS33	VSS33
W26	VSSAHT23	VSS34	VSS34
W21	VSSAHT24	VSS35	VSS35
W22	VSSAHT25	VSS36	VSS36
W25	VSSAHT26	VSS37	VSS37
W21	VSSAHT27	VSS38	VSS38
AD25	VSSAHT28	VSS39	VSS39
L12	VSSAHT29	VSS40	VSS40
M14	VSSAHT30	VSS41	VSS41
N13	VSSAHT31	VSS42	VSS42
P12	VSSAHT32	VSS43	VSS43
R11	VSSAHT33	VSS44	VSS44
T11	VSSAHT34	VSS45	VSS45
T12	VSSAHT35	VSS46	VSS46
U14	VSSAHT36	VSS47	VSS47
VSS20	VSSAHT37	VSS48	VSS48
W15	VSSAHT38	VSS49	VSS49
W16	VSSAHT39	VSS50	VSS50
VSS23	VSSAHT40	VSS51	VSS51
VSS24	VSSAHT41	VSS52	VSS52
VSS25	VSSAHT42	VSS53	VSS53
VSS26	VSSAHT43	VSS54	VSS54
VSS27	VSSAHT44	VSS55	VSS55
VSS28	VSSAHT45	VSS56	VSS56
VSS29	VSSAHT46	VSS57	VSS57
VSS30	VSSAHT47	VSS58	VSS58
AE20	VSSAHT48	VSS59	VSS59
VSS32	VSSAHT49	VSS60	VSS60
VSS33	VSSAHT50	VSS61	VSS61
VSS34	VSSAHT51	VSS62	VSS62
VSS35	VSSAHT52	VSS63	VSS63
VSS36	VSSAHT53	VSS64	VSS64
VSS37	VSSAHT54	VSS65	VSS65
VSS38	VSSAHT55	VSS66	VSS66
VSS39	VSSAHT56	VSS67	VSS67
VSS40	VSSAHT57	VSS68	VSS68
VSS41	VSSAHT58	VSS69	VSS69
VSS42	VSSAHT59	VSS70	VSS70
VSS43	VSSAHT60	VSS71	VSS71
VSS44	VSSAHT61	VSS72	VSS72
VSS45	VSSAHT62	VSS73	VSS73
VSS46	VSSAHT63	VSS74	VSS74
VSS47	VSSAHT64	VSS75	VSS75
VSS48	VSSAHT65	VSS76	VSS76
VSS49	VSSAHT66	VSS77	VSS77
VSS50	VSSAHT67	VSS78	VSS78
VSS51	VSSAHT68	VSS79	VSS79
VSS52	VSSAHT69	VSS80	VSS80
VSS53	VSSAHT70	VSS81	VSS81
VSS54	VSSAHT71	VSS82	VSS82
VSS55	VSSAHT72	VSS83	VSS83
VSS56	VSSAHT73	VSS84	VSS84
VSS57	VSSAHT74	VSS85	VSS85
VSS58	VSSAHT75	VSS86	VSS86
VSS59	VSSAHT76	VSS87	VSS87
VSS60	VSSAHT77	VSS88	VSS88
VSS61	VSSAHT78	VSS89	VSS89
VSS62	VSSAHT79	VSS90	VSS90
VSS63	VSSAHT80	VSS91	VSS91
VSS64	VSSAHT81	VSS92	VSS92
VSS65	VSSAHT82	VSS93	VSS93
VSS66	VSSAHT83	VSS94	VSS94
VSS67	VSSAHT84	VSS95	VSS95
VSS68	VSSAHT85	VSS96	VSS96
VSS69	VSSAHT86	VSS97	VSS97
VSS70	VSSAHT87	VSS98	VSS98
VSS71	VSSAHT88	VSS99	VSS99
VSS72	VSSAHT89	VSS100	VSS100
VSS73	VSSAHT90	VSS101	VSS101
VSS74	VSSAHT91	VSS102	VSS102
VSS75	VSSAHT92	VSS103	VSS103
VSS76	VSSAHT93	VSS104	VSS104
VSS77	VSSAHT94	VSS105	VSS105



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	RS880M-Power	DVT
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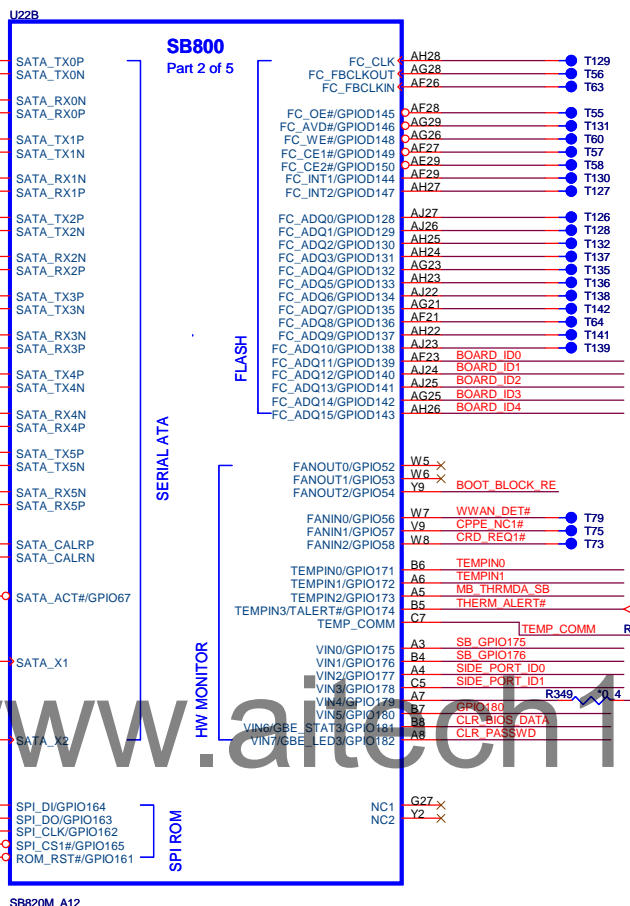
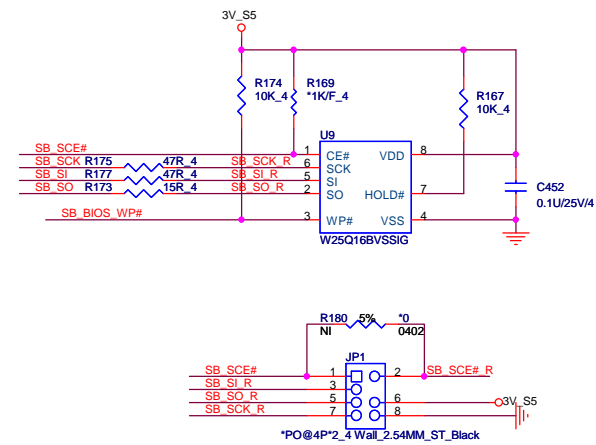
SATA HDD

SATA ODD

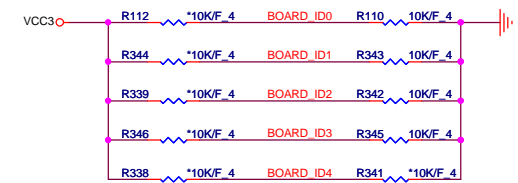
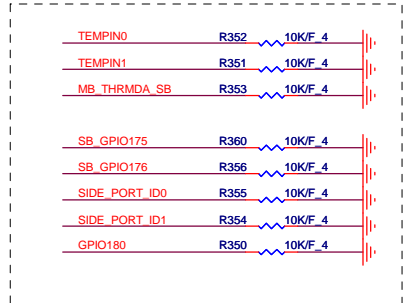
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800-? 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: TBD-? 1% resistor to GND. (1K ohm)
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

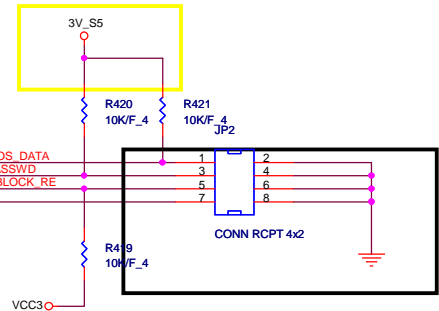
8Mbit, SPI



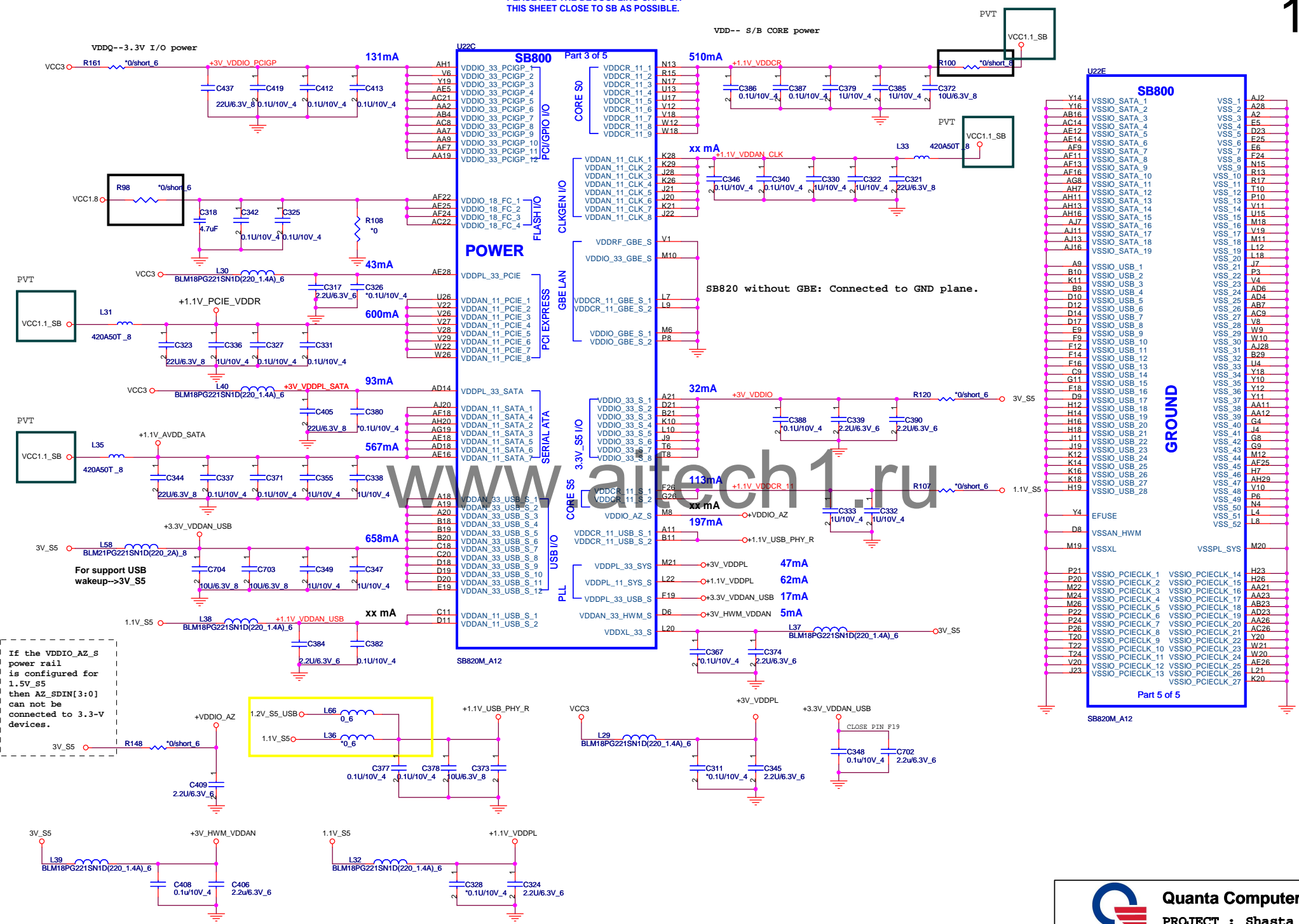
IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY



	ID4	ID3	ID2	ID1	ID0
0				UMA	
1				Discrete	



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



REQUIRED STRAPS

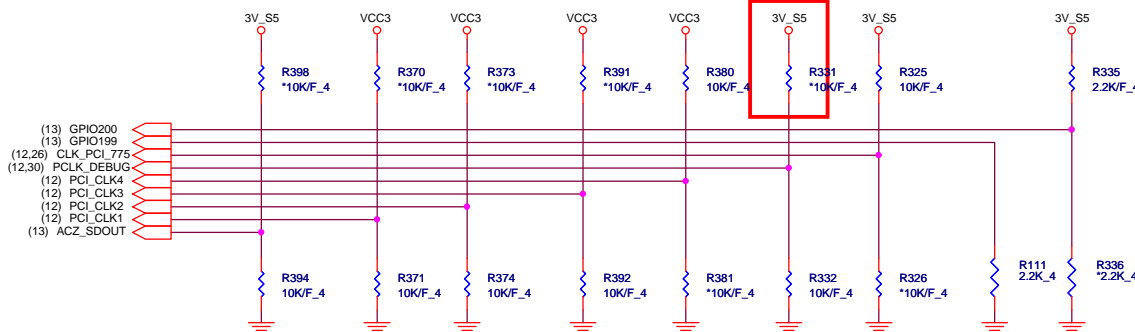


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

16

SB820M is supported Gen1 mode only.

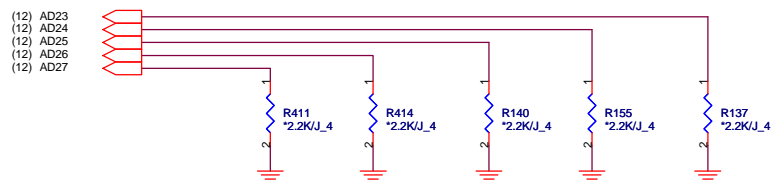
For internal clock GEN.



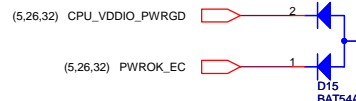
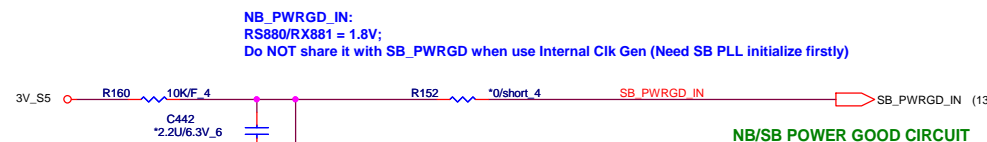
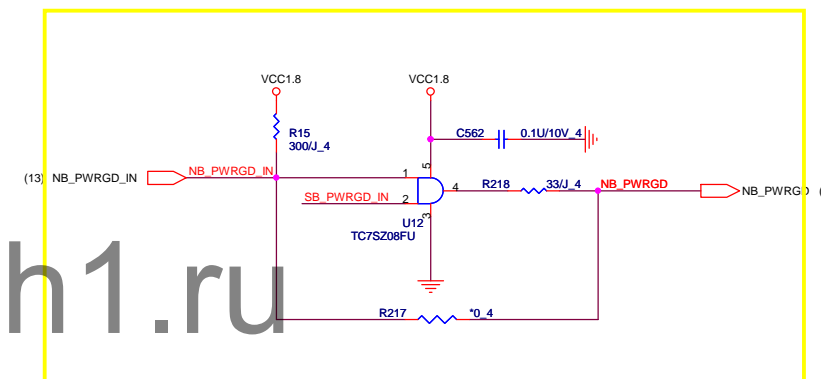
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE	EC ENABLED	INT. CLKGEN ENABLED	H, H=Reserved H, L=SPI ROM	DEFAULT
PULL LOW	PERFORMANCE MODE	FORCE PCIE Gen1	Watchdog Timer Disable	IGNORE DEBUG STRAPS	Fusion CLOCK MODE	EC DISABLED	EXT. CLKGEN ENABLE	L, H=LPC ROM L, L=FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT		DEFAULT			

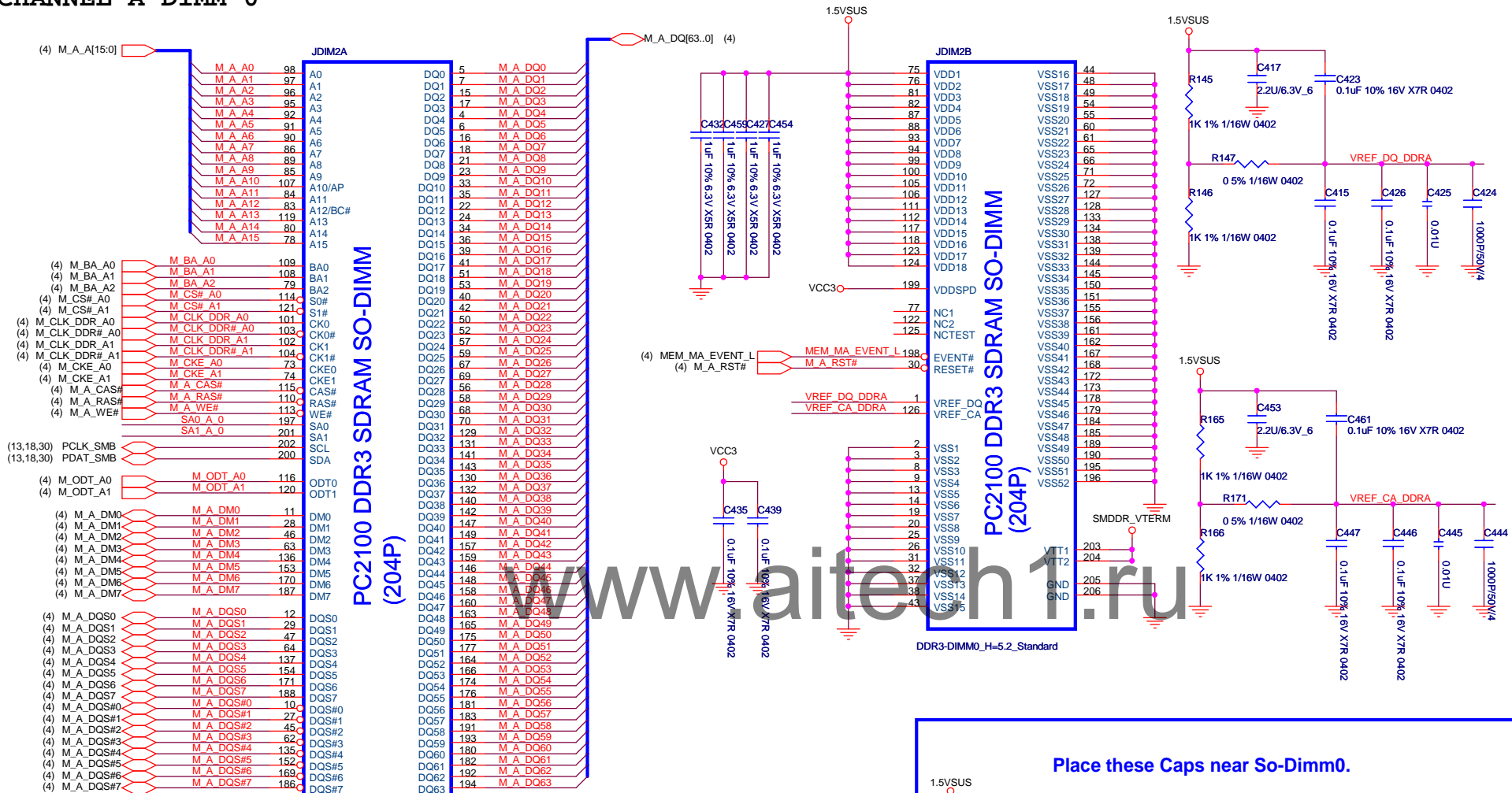
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	DISABLE I2C ROM	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT

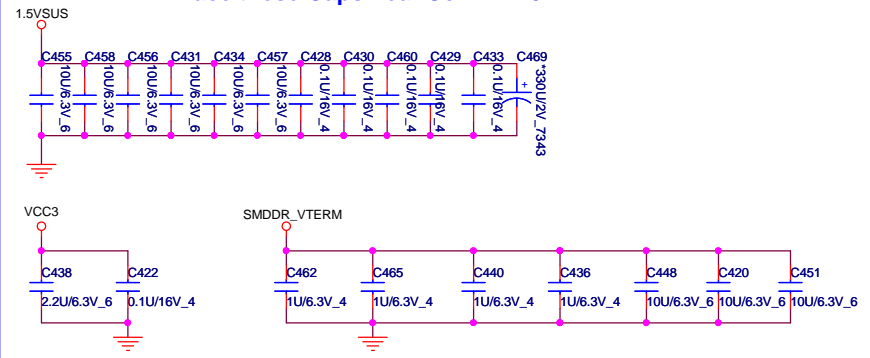




DDR3-DIMM0_H-5.2_Standard



Place these Caps near So-Dimm0.



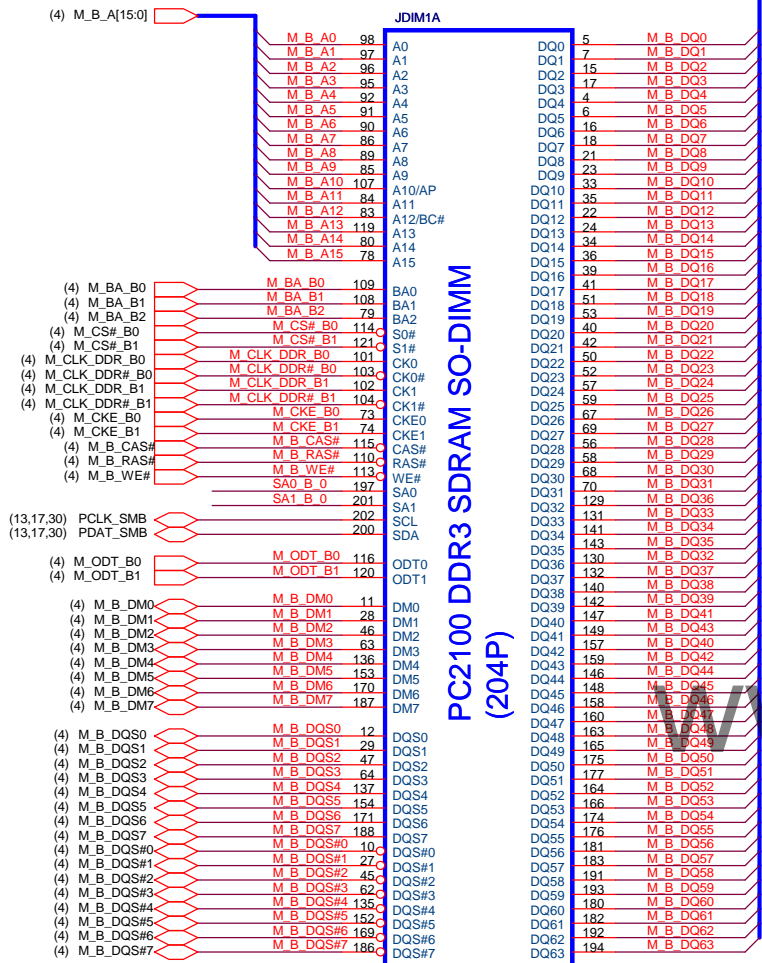
SPD SA0	0
SPD SA1	0



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PROJECT : Shasta_(NZ2)

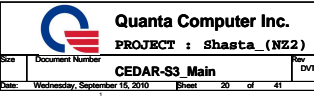
CHANNEL B DIMM 0

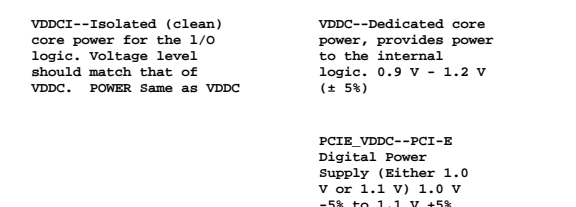
18

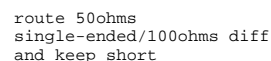
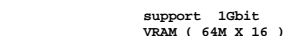




	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1V
M	0	1	0.95V
TBD	1	0	0.95V
L	1	1	0.9V

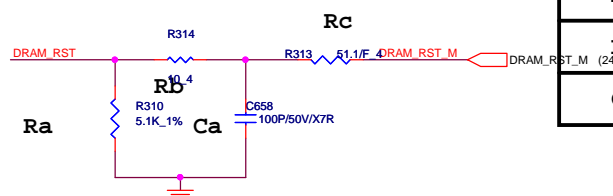
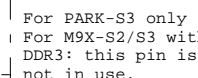






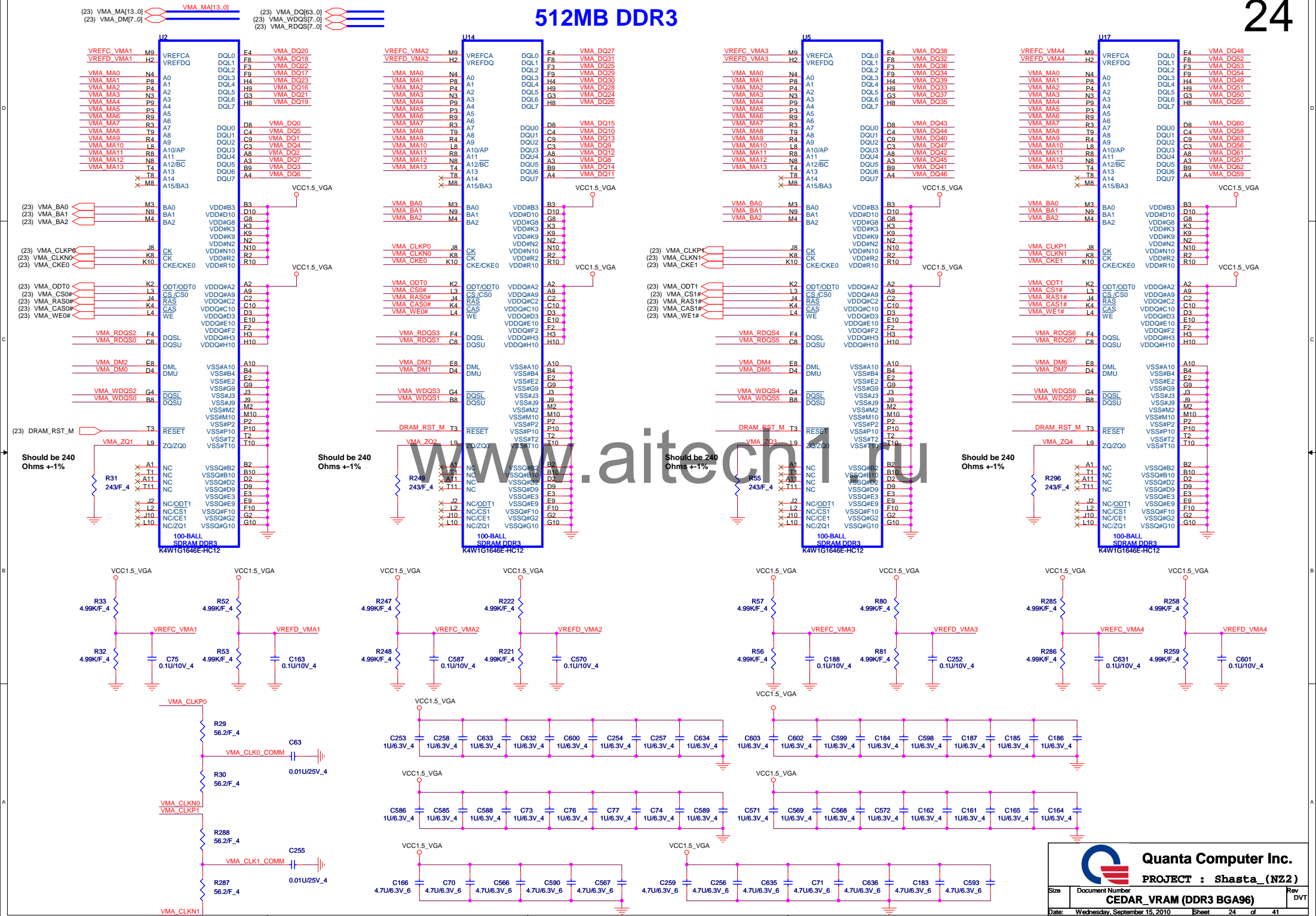
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

MEMORY INTERFACE

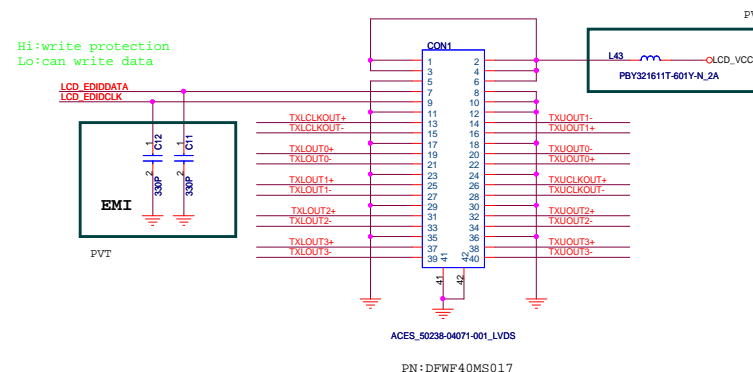


Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	680R
Rc	2.2K	DNI
Ca	2.2nF	68pF

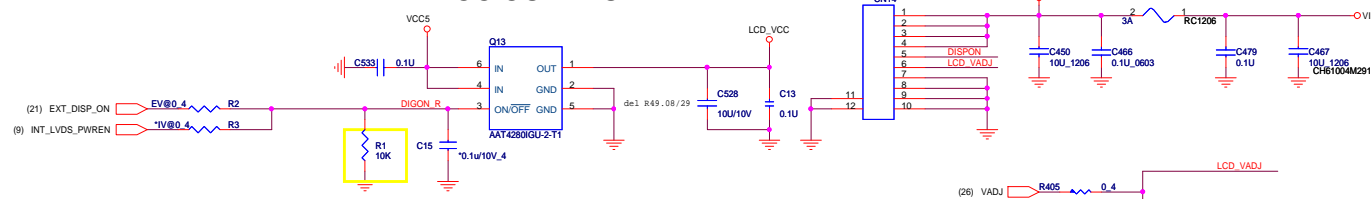
512MB DDR3



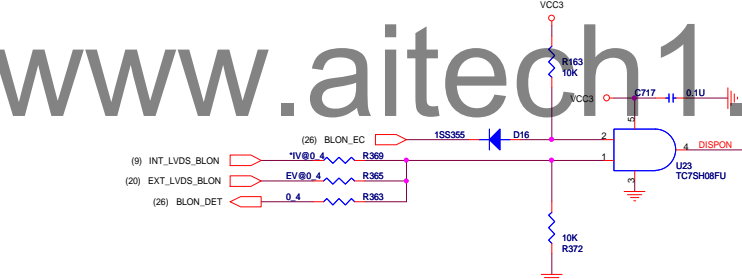
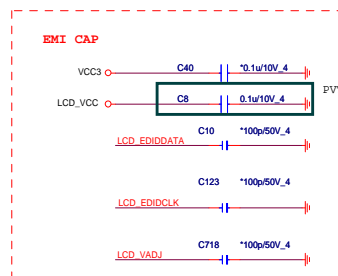
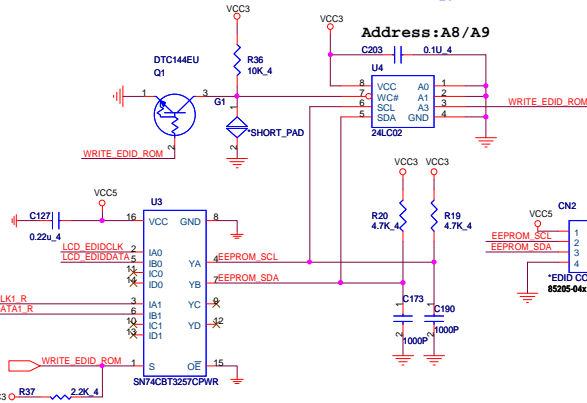
LCD CONNECTOR

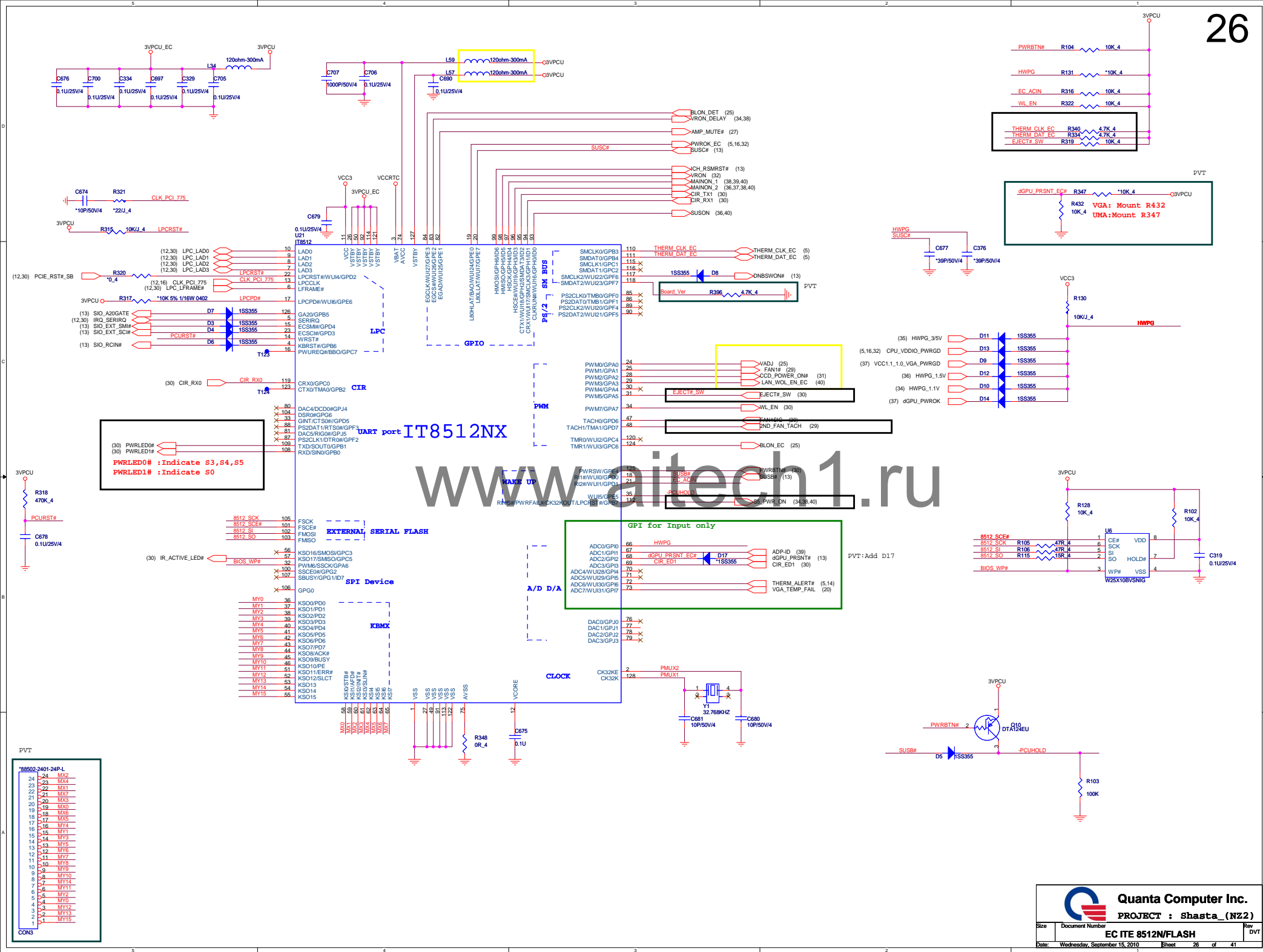


PANEL VCC CONTROL



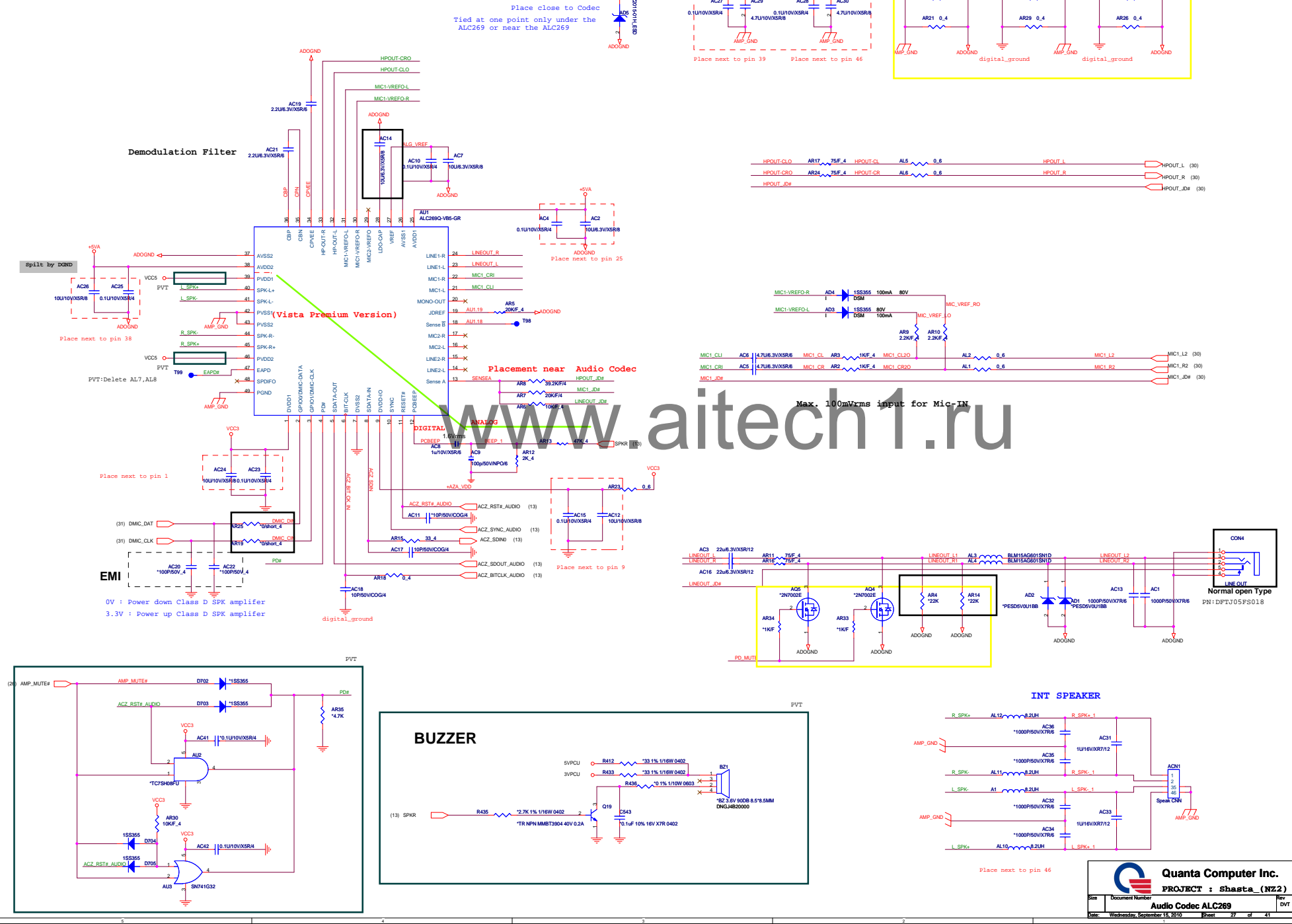
PANEL BACKLIGHT CONTROL

EEPROM IIC Selection
PANEL EDID DATA

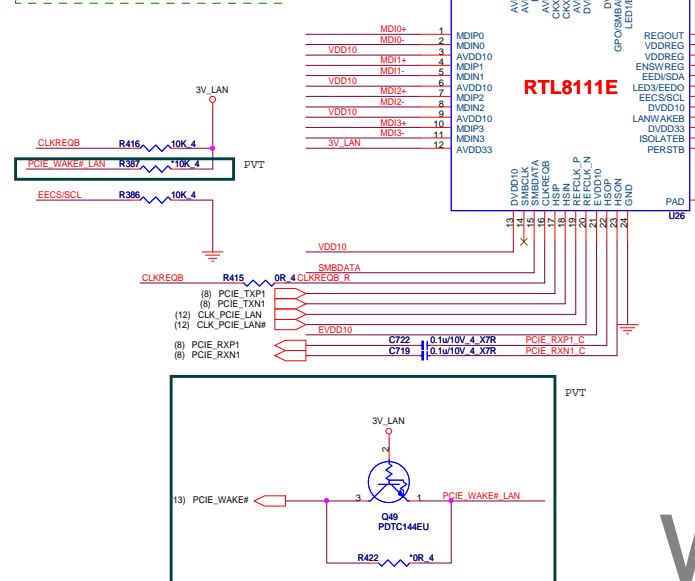


Codec ALC269QAFP-VB5-GR
Sonic Focus support.

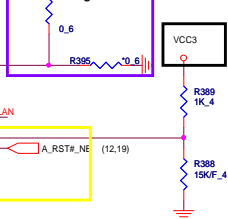
0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier



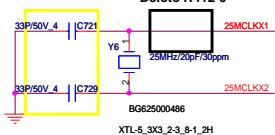
Using EFuse only without ASF function.



R23 For Enable Switch Regulator.
R24 For Disable Switch
Regulator.



Delete R412 0



3V3_LAN

R176 0.6

AVDD33_REG

C466 0.1u_4

C467 0.1u_4

C468 0.1u_4

C469 0.1u_4

C470 0.1u_4

C471 0.1u_4

C472 0.1u_4

C473 0.1u_4

C463 4.7u10V_6

Near pin 12,27,39,42,47,48

Close LAN chip pin 34,35

VDDIO

R172 0.6

4.7uH4850mA

REGOUT

C489 0.1uF_4

C487 0.1uF_4

C482 0.1uF_4

C488 0.1uF_4

C480 0.1uF_4

C483 0.1uF_4

C472 0.1uF_4

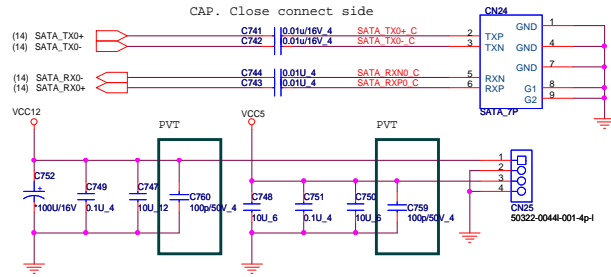
Near pin 3,6,9,13,29,41,45

C468 0.1uF_4

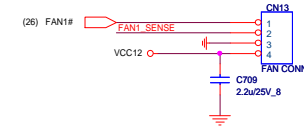
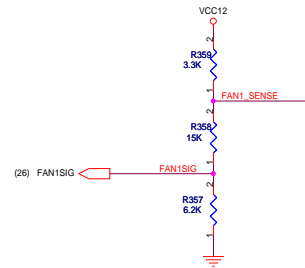
C464 4.7u10V_5

Close LAN chip pin 36

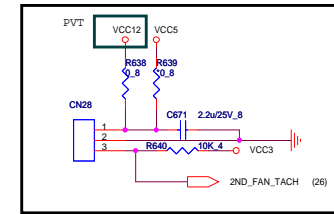
1st 2.5"/3.5" SATA HDD Wire Type



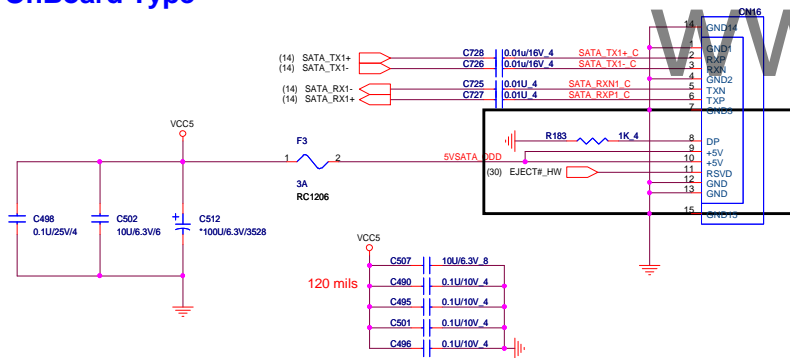
FAN CONN



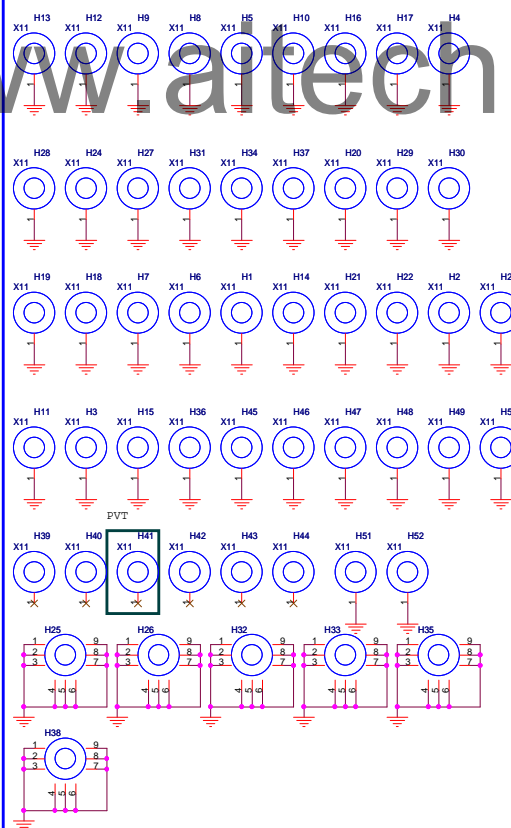
2nd FAN CONN



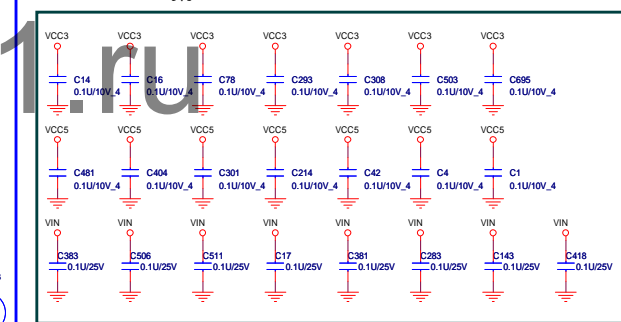
SATA CD-ROM OnBoard Type



HOLE

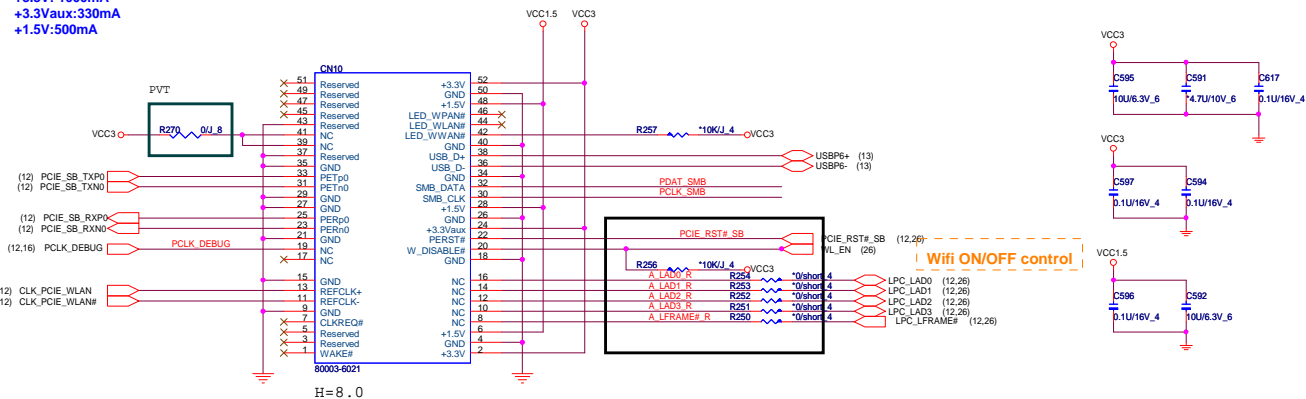


EMI CAP

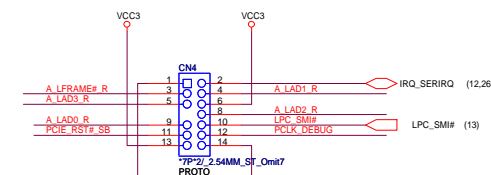


Wireless + BT

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

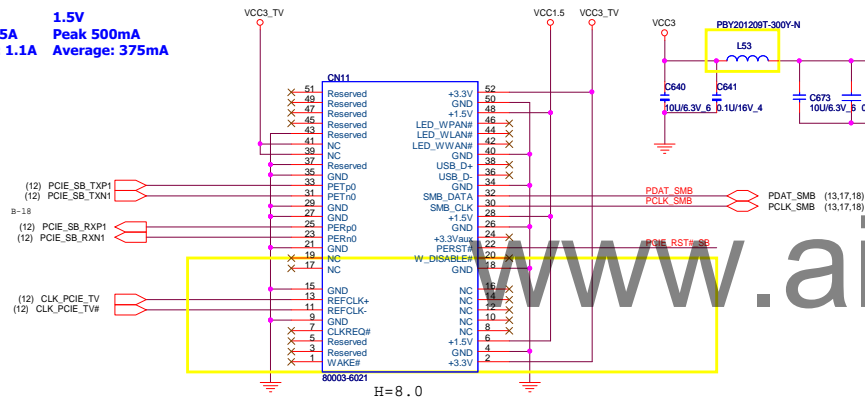


LPC HEADER

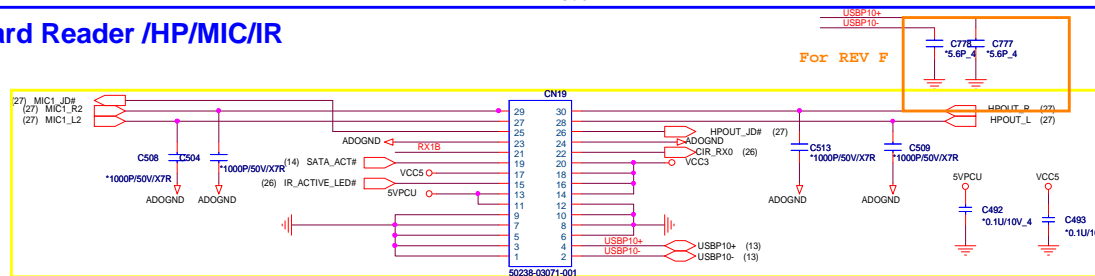


TV

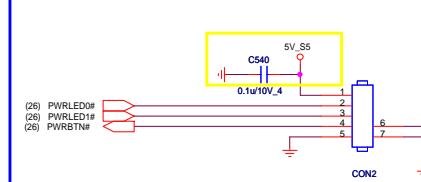
3.3V	1.5V
Peak 2.75A	Peak 500mA
Average: 1.1A	Average: 375mA



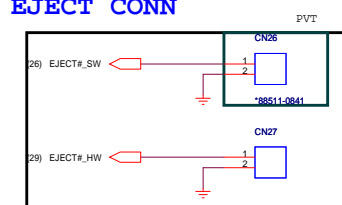
Card Reader /HP/MIC/IR



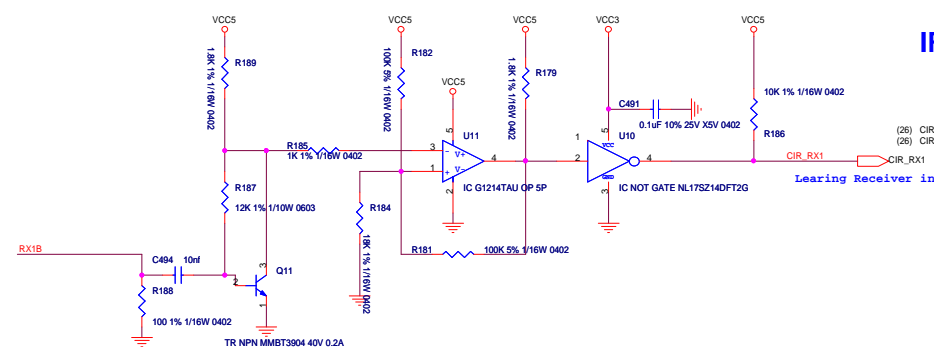
Power Button connector



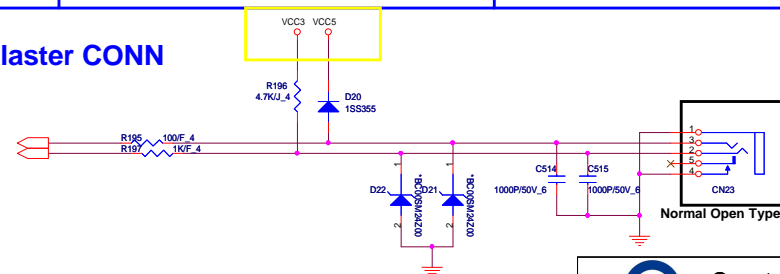
ODD EJECT CONN



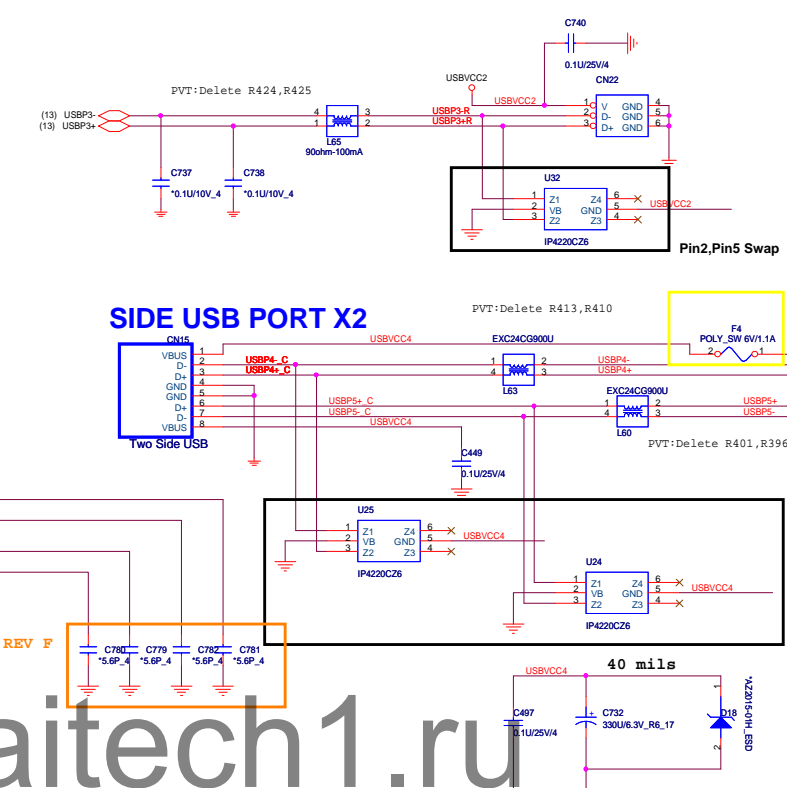
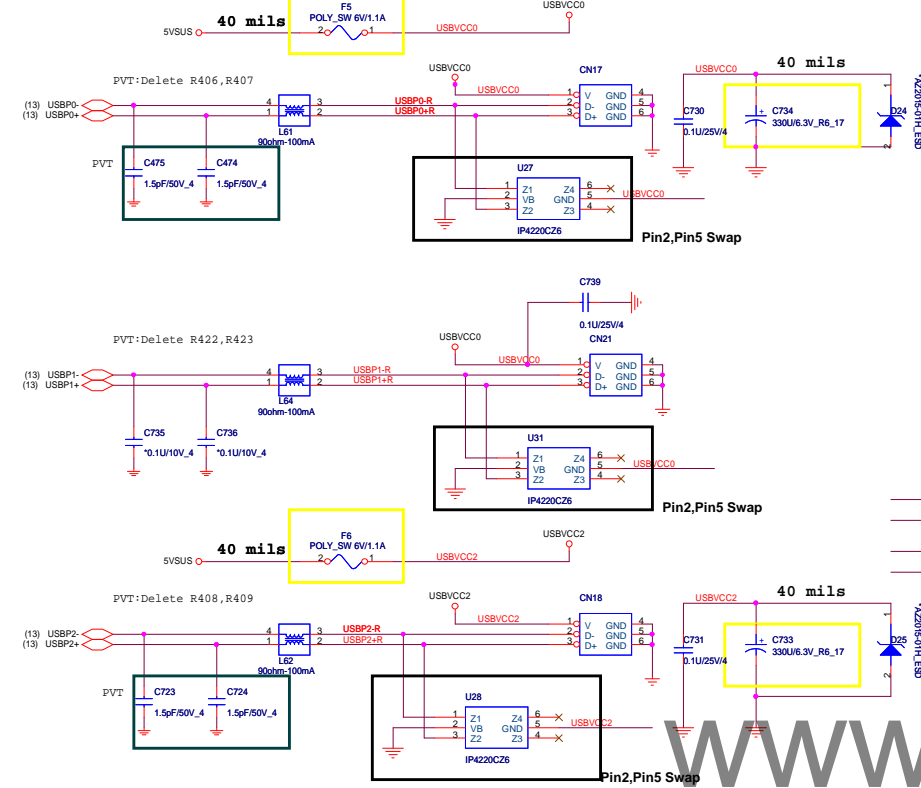
IR Blaster



IR Blaster CONN



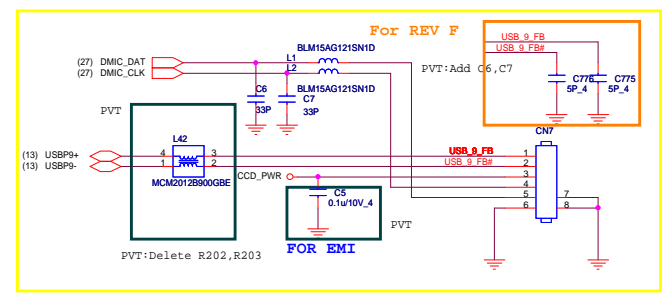
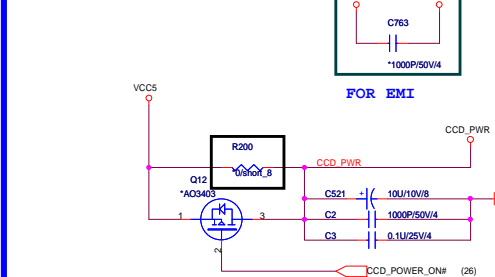
USB PORT X4



LED STATUS FOR DEBUG

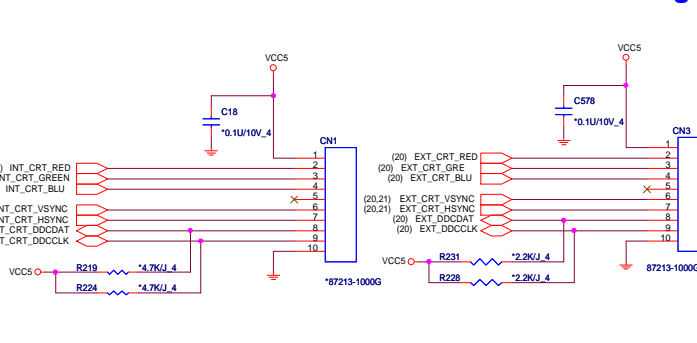
PR:Delete LED2,LED3,LED4,LED5,LED6,LED7,R426,R427,R428,R429,R430,R431,Q14,Q15,Q16,Q17,Q18

WEB CAM MODULE

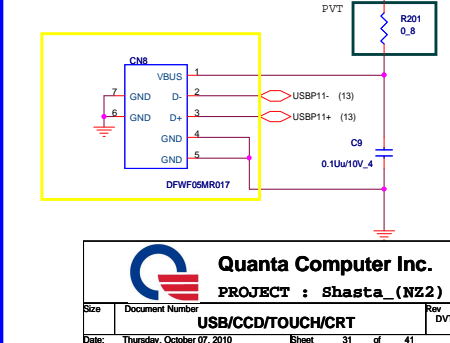


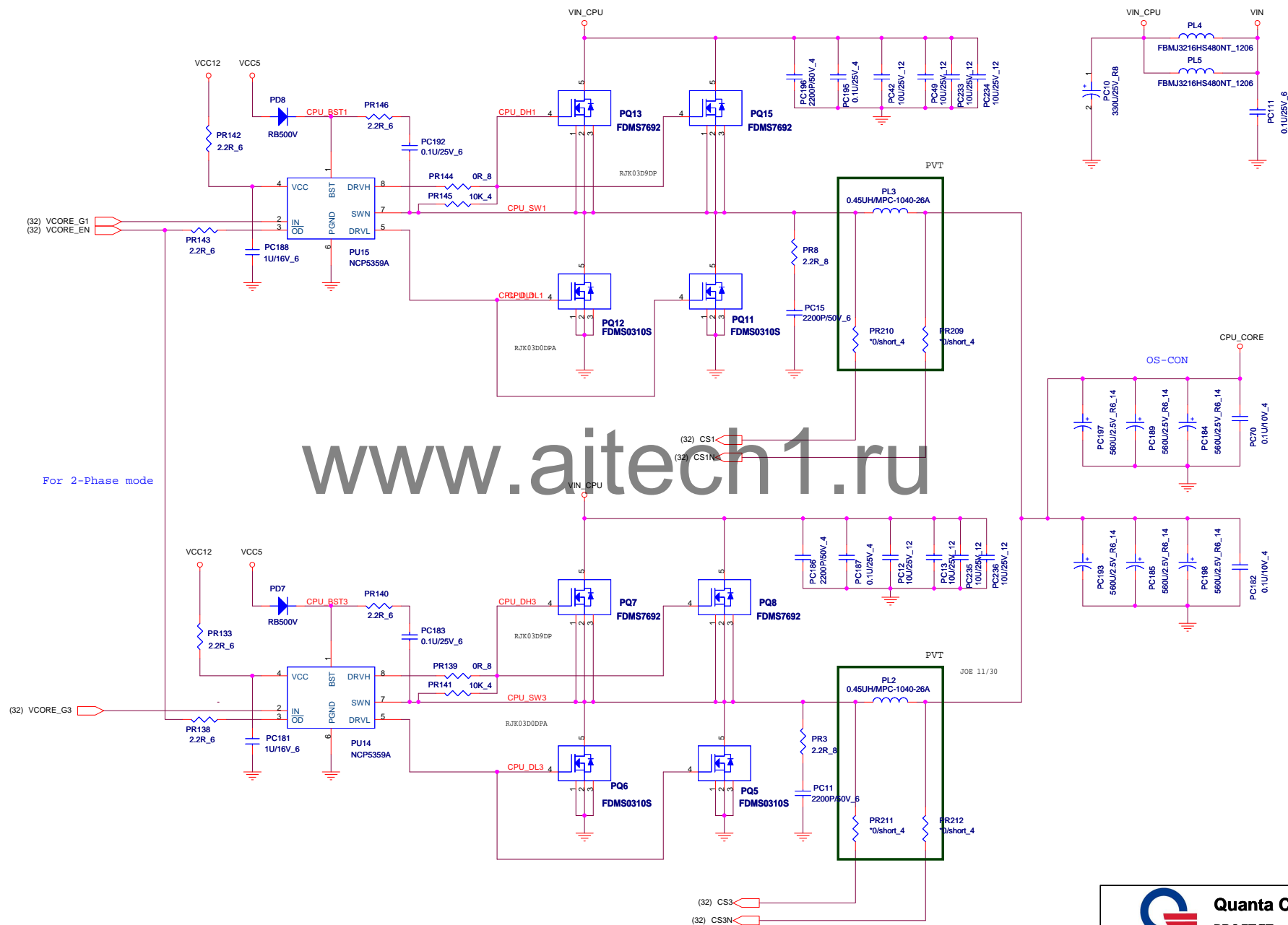
UMA CRT FOR DEBUG

Discrete CRT for Debug

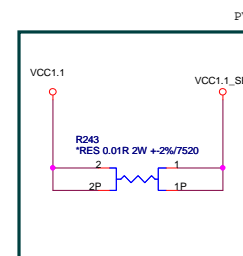
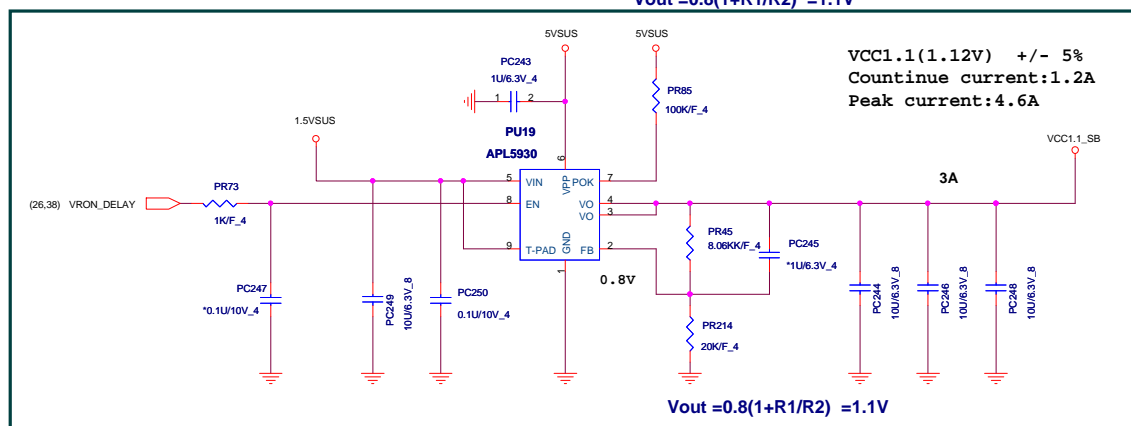
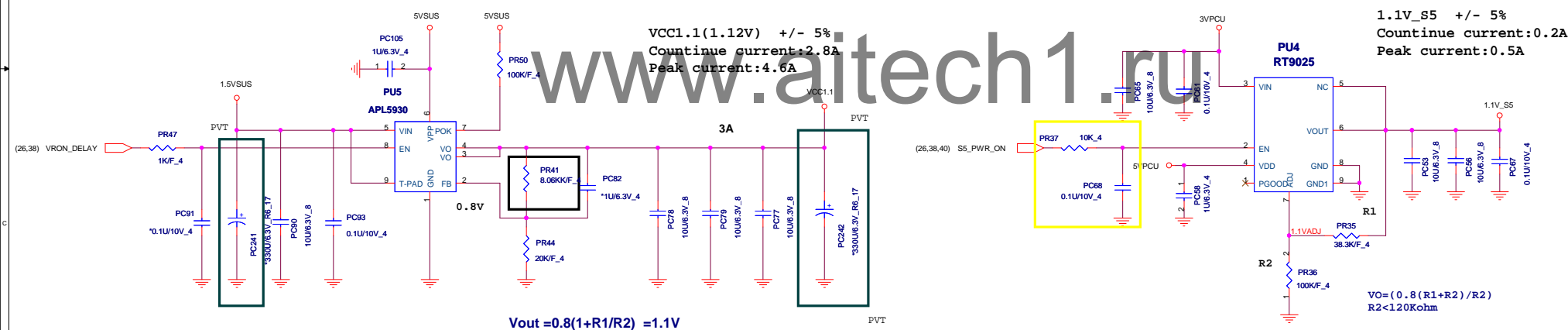
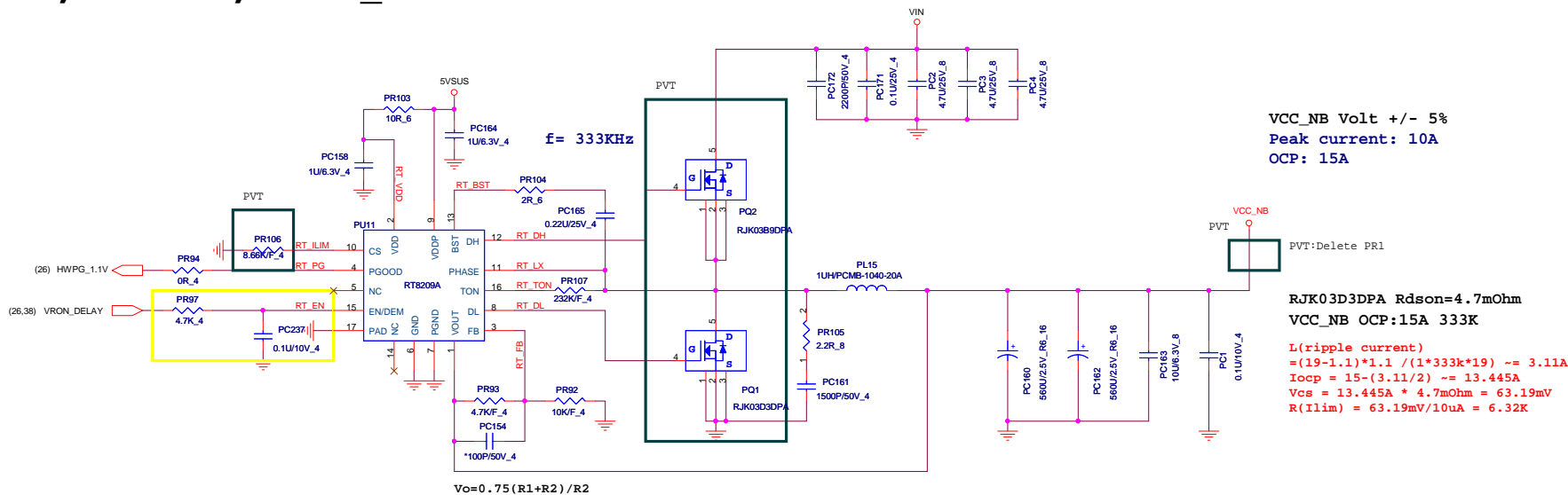


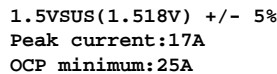
Touch Panel connector





NB_CORE, VCC1.1, 1.1V_S5

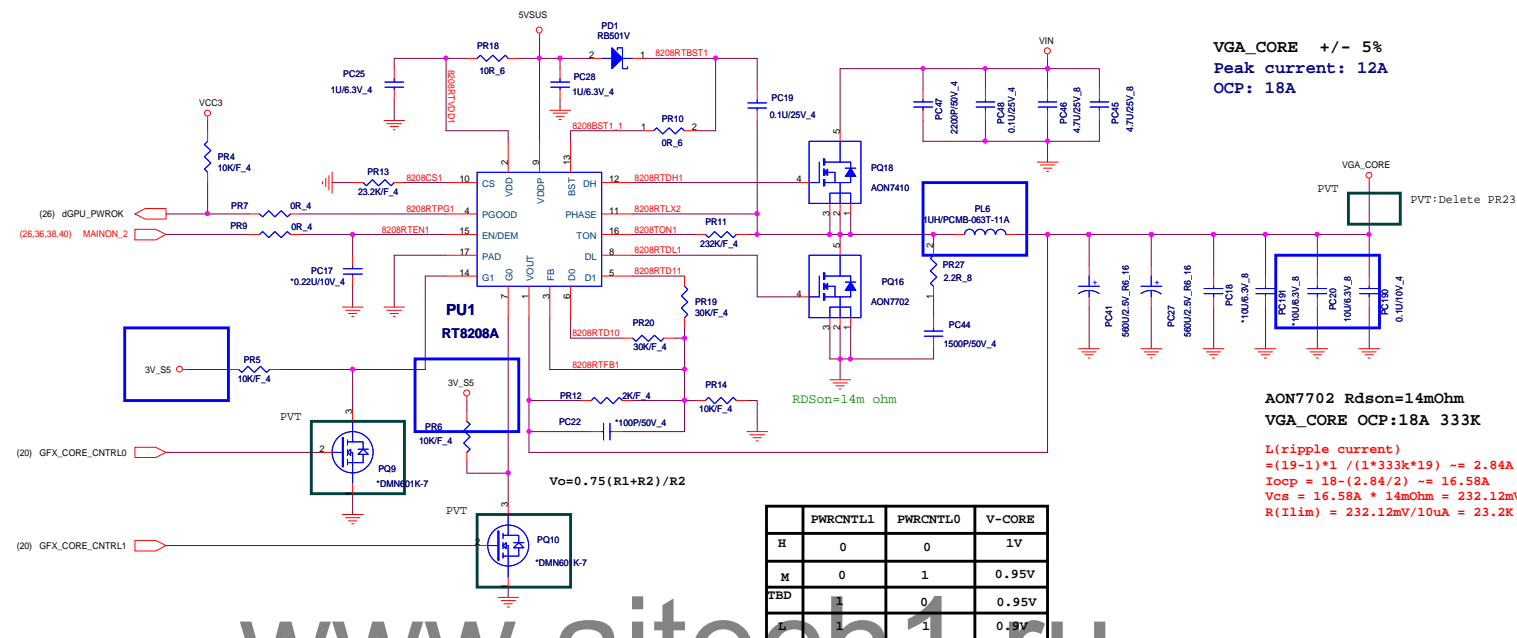




1.5VSUS OCP:25A 400K

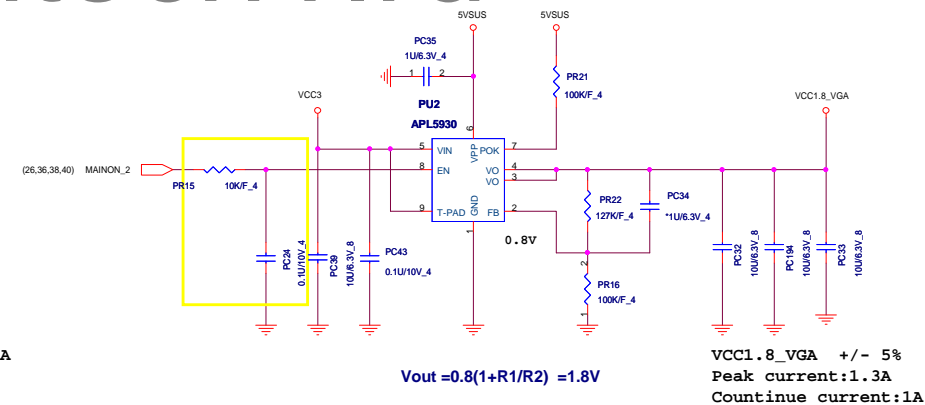
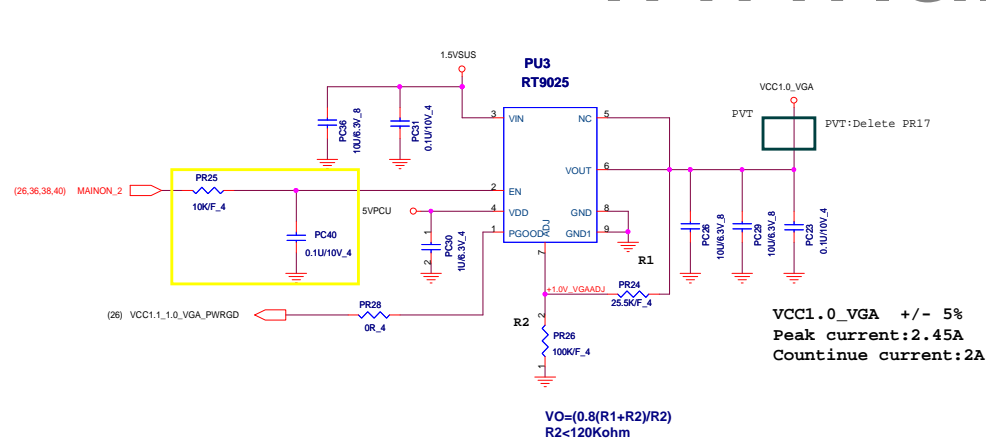
$$\begin{aligned} I_{ocp} &= 25 - (3.45/2) = 28.275A \\ V_{trip} &= 28.28A * 2.15m\Omega = 60.8mV \\ R_{trip} &= 60.8mV / 10\mu A = 6.08K \end{aligned}$$

VGA Core

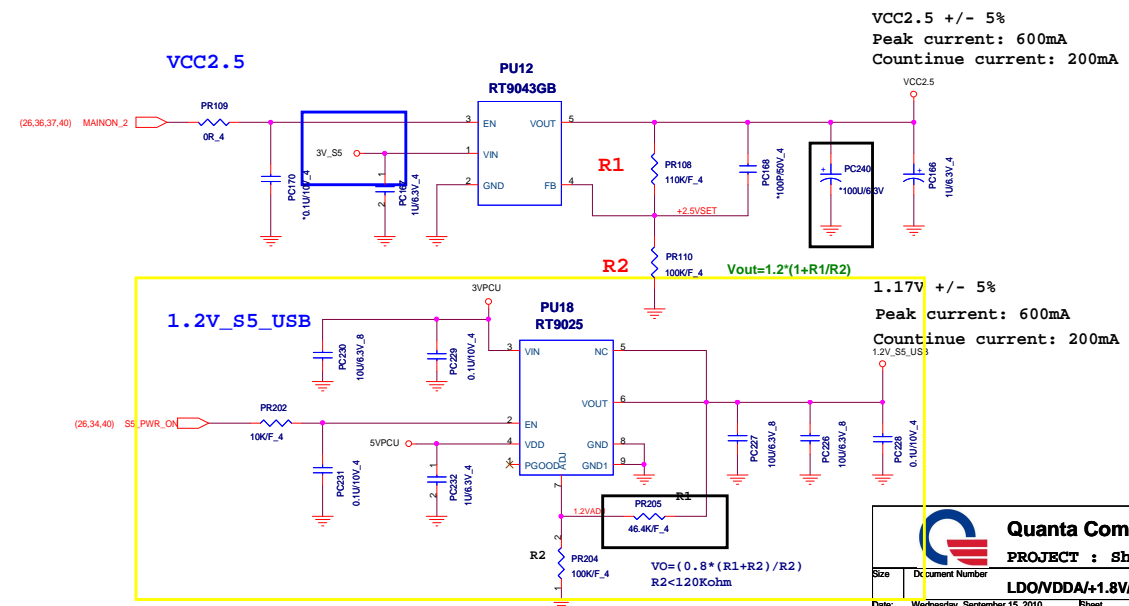
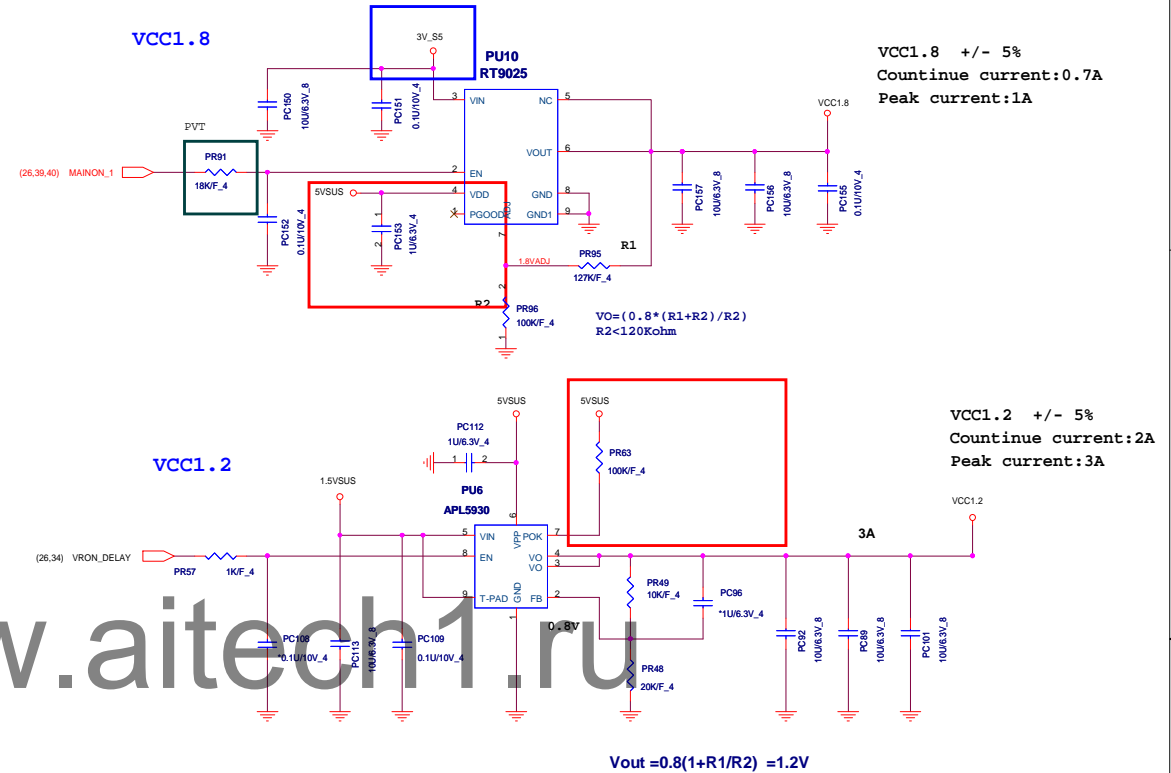


	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1V
M	0	1	0.95V
TBD	1	0	0.95V
L	1	1	0.9V

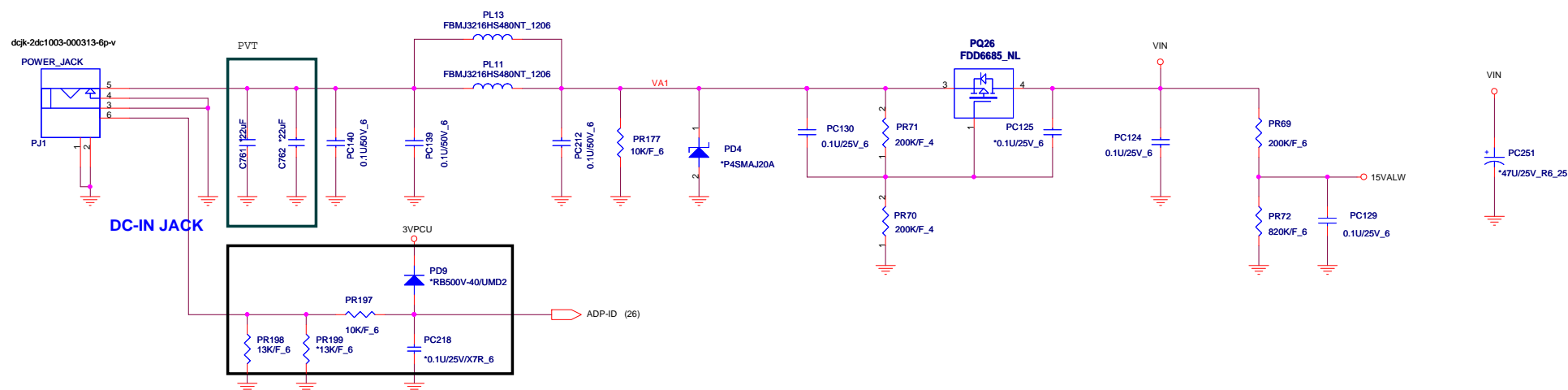
TBD	1	0	0.95V
L	1	1	0.9V



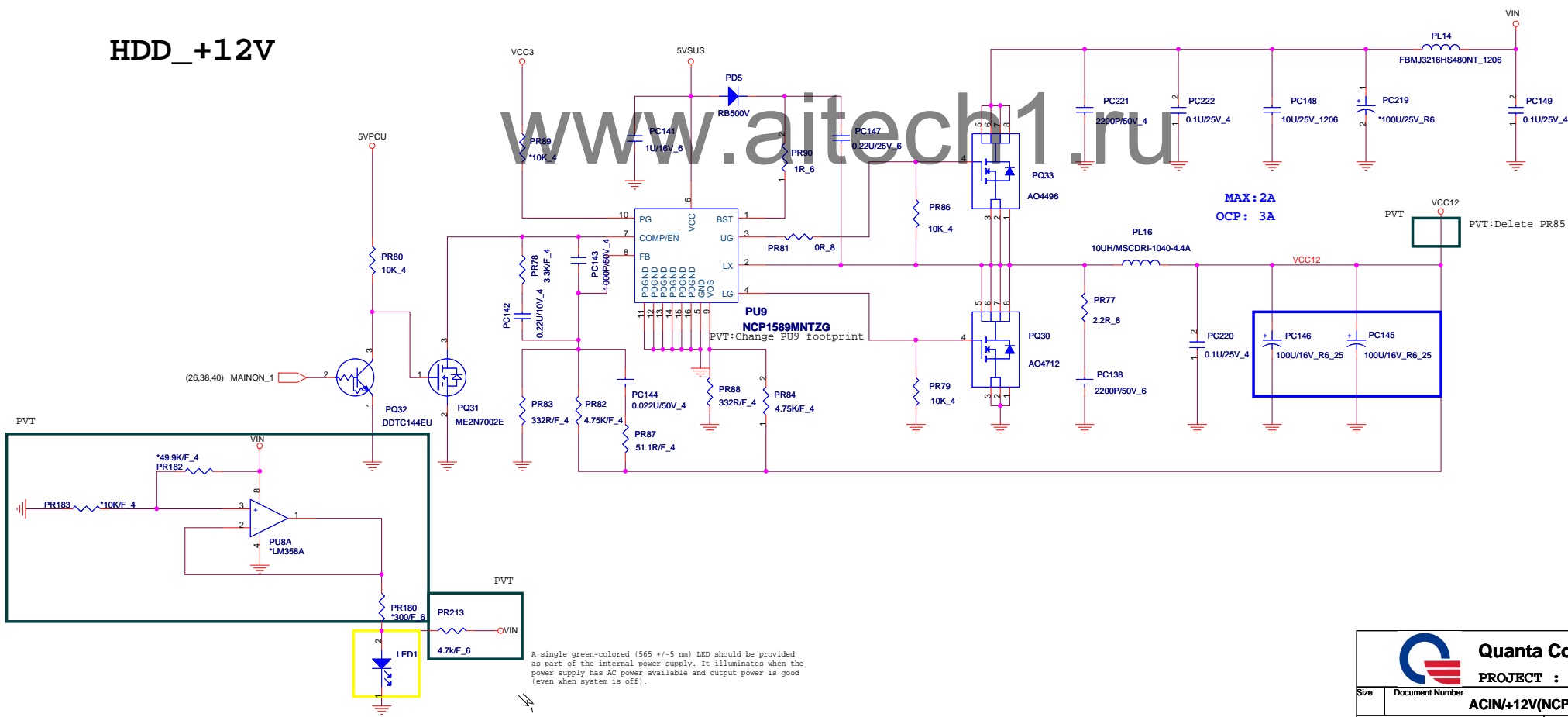
VCC1.8, VCC1.2, VDDNA (2.5V)



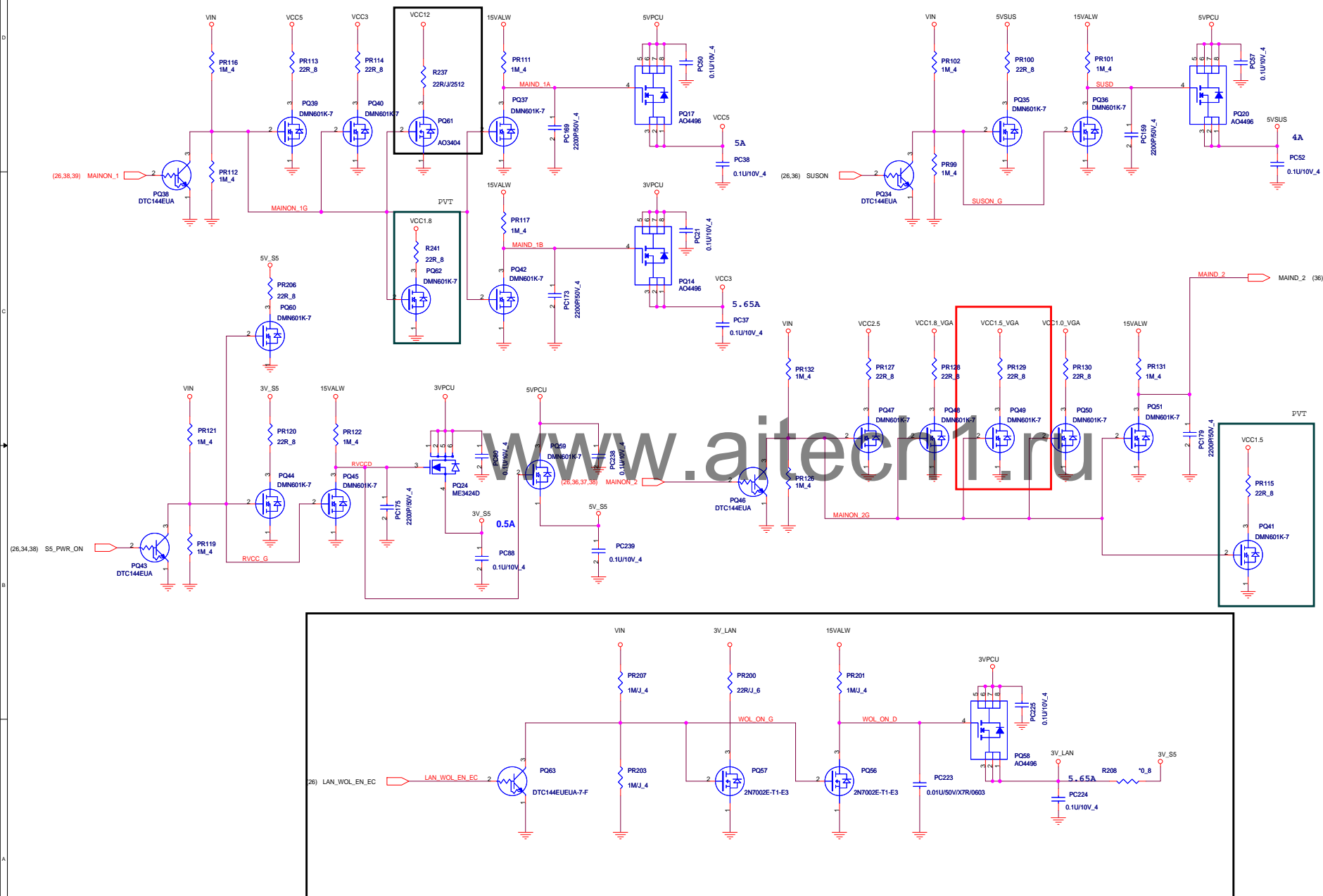
DC IN JACK



HDD_+12V




Discharge, Mosfet SW



- 1.Add R208(RC0603).
- 2.Mount PR197,PR198(ADP-ID circuit).
- 3.PR205 Change to 46.4K(USB PHY 1.17V).
- 4.Change footprint R250,R251,R252,R253,R254,R200,R76,R89,R62,R213,R98,R65,AR19,AR25,R202,R203.
- 5.Delete R255,R412,U7,R237,R241,R243,G2 PAD,L4.
- 6.AddCN27 (ODD_Eject for HW).
- 7.Add CN16 Pin11 net for Eject#_HW behavior.
- 8.Change AR30,AR31 Power to VCC3.
- 9.Add Clear_CMOS to JP2 pin 7.
- 10.Reserve PC240.
- 11.Change PL6 P/N a DC-10B0M007.
- 12.Change PC145, PC146 P/N a CC71003MZ11.
- 13.Change PR195 a4.99K/1%_0402 aCS24992FB26.
- 14.Mount PC20.
- 15.Change PR175 a 2K/1%_0405 a CS22002FB19.
- 16.Change PL16, PL7, PL8 footprint a choke-etqp4lr36wfc-smt.
- 17.Add PU18 RT9025 for 1.2V_S5_USB.
- 18.Change PC10, PC16 a 100uF/25 (CC71004MZ04) to PC10 a 330uF/25V (CC73304MZ29).
- 19.Remove PC6, PC14, and change PC42, PC49, PC12, PC13 a 4.7uF/25V (CH5474MEA07) to 10uF/25V (CH61004M291).
- 20.Mount AC14.
- 21.Del AQ4, AQ5, AR33, AR34, AR4, AR14.
- 22.Add VCC12 Discharge circuit PQ61, R237.
- 23.change PC240 a 100uF/6.3V a CH71001M687.
- 24.U24,U25,U27,U28,U31,U32 USB ESD IC Pin2,Pin5 swap.
- 25.Move S5_PWR_ON net form EC 90 pin to 112pin.
- 26.PQ1,PQ2 footprint change.
- 27.PR187 change to 76.8K CS37682FB00.
- 28.PR41 change to 8.06K CS28062FB21.
- 29.R100 footprint modify.
- 30.CON4,CN23 footprint modify
- 31.Connect R389 to VCC3
- 32.Add CN28,C671,R640,R638,R639
- 33.Change PWRLED0#,PWRLED1# to EC pin108,109 from pin48,120
- 34.Reserve R63,mount R71
- PVT:
- 35.Change PL1,PL2,PL3 footprint,Add PR98,PR208,PR209,PR210,PR211,PR212
- 36.Add Buzzer BZ1,R435,Q19,C543,R436,R433,R412
- 37.Delete AR30,AR31,AQ1,AQ2,AQ3,AddD702,D703,AC41,AU2,AR35
- 38.Change PQ1,PQ2 to RJK03D3DPA & RJK03B9DPA
- 39.Delete AL7,AL8
- 40.Delete PR1,PR34,PR45,PR73,PR23,PR17,PR85
- 41.VCC1.5 Discharge connect to MAINON_2
- 42.Delete R406,R407,R422,R423,R408,R409,R424,R425,R410,R413,R401,R396,R202,R203
- 43.Change PU16 footprint
- 44.Change PR106 to 8.66k
45. Add R396,D17
- 46.2nd Fan R638 connect to VCC12 from VCC3
- 47.Reserve C745,C748,C757,C758,C756,C716 for EMI request
- 48.Add C14,C16,C78,C293,C308,C503,C695,C481,C404,C301,C214,C42,C4,C1,C383,C506,C511,C17,C381,C283,C143,C418 for EMI request
- 49.Add C5,C6,C7,L42
- 50.R201 change to bead
- 51.Add C759,C760 for EMI request
- 52.Reserve for C761,C762,C763 for EMI request
- 53.Reserve R387,R422,Add Q49
- 54.Add PC241,PC242
- 55.Add C8,C11,C12
- 56.Add and Reserve R401,Reserve PQ9,PQ10
- 57.Delete R10
- 58.Add C764,C765,C766,C767
- 59.Mount R270
- 60.PC85 change to 10uF
- 61.Change PU9,PU16 footprint
- 62.Add R241,PQ62
- 63.Add C769,C771,C772,C773,C770,C768 for EMI
- 64.Add D704,AC42,AU3
- 65.Add C774
66. Add PR213,Reserve PU8,PR182,PR183,PR180
- 67.Add PU19,PC243,PR85,PR73,PC247,PC249,PC250,PR45,PR214,PC245,PC244,PC246,PC248
68. Reserve R243
69. Add AR30,D705
- 70.Mount C474,C475,C723,C724
71. Reserve CN5,CON3
72. Reserve CN26
73. Delete LED2,LED3,LED4,LED5,LED6,LED7,R426,R427,R428,R429,R430,R431,Q14,Q15,Q16,Q17,Q18
74. Add C780,C779,C782,C781,C776,C775,C778,C777 for USB D+/D-

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		Quanta Computer Inc.	
		PROJECT : Shasta (NZ2)	
Size	Document Number	Rev DVT	
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Date	Friday, September 17, 2010	Sheet	41 of 41